A. Honors Structure: Semiconductor IC Technology.

Sr. No.	Course Code	Courses Name	Sem	Hours per week			Credit	Examination Scheme					Total
				L	T	P		ISE	ESE	TW	PR	OR	
1	ETHDT511	Semiconductor technology overview	V	3	-	-	3	40#	60*	-	-	-	100
	ETHDT512	Basic Semiconductor Technologies lab	V	-	-	2	1	-	-	-	-	25	25
2	ETHDT613	Assembly, Test, Marking and packaging (ATMP) of Integrated circuits.	VI	3	-	-	3	40#	60*	-	-	25	100
	ETHDT614	ATMP basic lab	VI	-	-	2	1	-	-	-	-	25	25
3	ETHDT707	Semiconductor Wafer Fabrication.	VII	3	-	-	3	40#	60*	-	-	-	100
	ETHDT708	Semiconductor Processing lab	VII	-	-	4	2	-	-	25	-	25	50
4	ETHDT803	Semiconductor Integrated circuit design	VIII	3	-	-	3	40#	60*	-	-	-	100
	ETHDT804	Integrated Circuit Design Lab	VIII	-	-	4	2	-	-	25	-	25	50
			Total	12	-	12	18	160	240	50	-	100	550

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Third Year Electronics and Telecommunications (2022 Course) Semiconductor technology overview ETHDT511			
Course Code:	**ETHDT511**	**Credit**	**3**
Contact Hours:	3 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Examination: 40 Marks	End-sem. Examination: 60Marks	

Pre-requisites: Basic Mathematics,Semiconductor Physics

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-sem. Examination	Internal	40
2.	End Semester Examination	External	60

Course Objectives	
1	To provide a high level semiconductor overview.
2	To build basic understanding of honors degree modules to be covered in subsequent semesters.
3	To Demonstrate selected processes in semiconductor technology through labs and develop student interest.
4	To Understand semiconductor global supply chain.

Course Outcomes: Students will be able to	
511.1	Recall key semiconductor physics concepts and historical milestones.
511.2	Appreciate test concepts and acknowledge the need for good test coverage
511.3	discuss wafer fabrication process flow
511.4	Discuss current technology trends and improvements over historical process.
511.5	Explain Understand global semiconductor supply chain.

Topics covered:
UNIT I: Semiconductor process overview
From design to tested package process overview, Active and passive components, Limitations, IC types by sector, application and design
UNIT II: Packaging, Assembly and marking overview.
Packaging process, material required, Types of packages, Need for marking, marking process, Marking information and traceability.
UNIT III:Test development and testing overview.
How data sheets and test programs are related, Test development process flow, test verification, first silicon, yield improvement, production program for wafer test, package test and QA tests.
UNIT IV:Wafer fabrication overview
Raw material, ingot making, wafer slicing, oxidation, photolithography, etching, deposition, ion implantation, diffusion, cleaning, metalization, chemical mechanical polishing, ET testing, wafer packing.
UNIT V: IC design overview
Overview of system specification, architecture design, functional design, logic design, circuit design, physical design, physical layout, design rule check, Layout vs schematic, Tape out.

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Text Books:

1. Semiconductor Physics and Devices: Basic Principles by Donald A. Neamen - r.
2. Solid State Electronic Devices by Ben G. Streetman and Sanjay Kumar Banerjee -

Reference Books:

1. Handbook of Semiconductor Manufacturing Technology by Yoshio Nishi (Editor); Robert Doering (Editor)
2. Fundamentals of Semiconductor Materials and Devices, Adrian Kitai

3.Integrated circuits: Design, Fabrication and testing. Peter Shepherd. Red Globe Press.

E- Books / E- Learning References:

1. **https://www.youtube.com/watch?v=QpSr2OQdCfQ**
2. **https://www.youtube.com/watch?v=kQBqOdzNf6g**

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Third Year Electronics and Telecommunications (2022 Course) Basic Semiconductor Technologies Lab ETHDT 512			
Course Code:	**ETHDT512**	**Credit**	**1**
Contact Hours:	2 Hrs/week (L)	**Type of Course:**	Practical
Examination Scheme	Oral 25 Marks		

Pre-requisites:Semiconductor basics.

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	Oral Examination	External	25

Course Objectives

1	To educate students on parts of the cleanroom and definitions.
2	To understand the procedure required to enter and exit a cleanroom.
3	To appreciate and understand types of chemicals and glasses used in the process.
4	To demonstrate the package decapsulation process to view internal structure

Course Outcomes: Students will be able to

512.1	Identify various materials, its sources and properties required in the semiconductor domain.
512.2	Explain types of cleanroom and its entry and exit requirements.
512.3	Differentiate various types of gloves, safety gears used in semiconductor material handling.
512.4	explain wafer orientation, notch location and types
512.5	Gain skills to decapsulate an integrated circuit package for analysis.

List of experiments:

1. Understand the semiconductor supply chain and observe materials used in the process physically
2. Observe a Cleanroom model and overview and understand rules to follow
3. To demonstrate the procedure of entering a cleanroom (Structure,exit plan, gown wearing)
4. To understand and types of gloves and understand the uses with chemicals
5. Decapsulate a packaged IC to view the internal structure
6. To thoroughly understand different Chemicals and gasses and safety precautions
7. To understand types of Si wafers (orientation, doping, sizes).
8. Develop a simple digital IC test program using design output files and data sheet

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Third Year Electronics and Telecommunications (2022 Course) Assembly, Test, Marking and packaging (ATMP) of Integrated circuits, ETHDT613			
Course Code:	**ETHDT613**	**Credit**	**3**
Contact Hours:	3 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Examination: 40 Marks	End-sem. Examination: 60Marks	

Pre-requisites:Semiconductor physics.

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-sem. Examination	Internal	40
2.	End Semester Examination	External	60

Course Objectives	
1	Provide students with a broad understanding of the semiconductor assembly process.
2	Demonstrate overall assembly process for semiconductor packaging.
3	Explain details of substrate design, packaging trends and quality aspects
4	Provide students with broad understanding of test development and testing of semiconductor integrated circuits.

Course Outcomes: Students will be able to	
613.1	Differentiate between different types of semiconductor IC packages..
613.2	Know the IC bill of material.
613.3	Appreciate the importance of quality and reliability.
613.4	Understand types of tests with respect to types of IC.
613.5	Gain broad understanding of post wafer test operations.

Topics covered:

UNIT I: Package development

Need for packaging, Package types, Thermal Design consideration, Package bill of materials. Substrate design consideration for flip chip packages.

UNIT II:Integrated circuit assembly

Wafer saw process and machines, Die attach process, materials and machines, Wire bonding process, material and machines, Marking process.

UNIT III: Package quality and reliability.

Reliability testing, Burn in testing, high temperature testing, temperature cycling, Failure analysis, Physical analysis, Packaging trends, 2d, 3d and multichip designs.

UNIT IV:Integrated circuit test development

Need for testing, Automatic Test equipment, Types of tests by IC type, Using design files to develop a test program, Inked & inkless wafer map generation, Wafer retest & yield criterion, Yield enhancement through test defect analytics

UNIT V:Integrated circuit testing.

Production testing, Temperature testing, wafer test and package test coverage, Test sockets, Probe cards, Probing machines, Package DUT testing board, Package test handlers. Trays, tubes, good and reject part separation,

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Text Books:

1.integrated circuits: Design, Fabrication and testing. Peter Shepherd. Red Globe Press.

Reference Books:

1.Semiconductor Packaging: Andrea Chen, Randy Hsiao, CRC Press.

2.Integrated Circuit Packaging, Assembly and Interconnections:William Greig, Springer publication.

3.Integrated circuit Test engineering: Ian A. Grout, New age international.

E- Books / E- Learning References:

1. https://www.youtube.com/watch?v=V9qhhko0s-w
2. https://www.youtube.com/watch?v=HdcLRMv3D3g

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Third Year Electronics and Telecommunications (2022 Course) ATMP Basic Lab ETHDT 614			
Course Code:	**ETHDT614**	**Credit**	**1**
Contact Hours:	2 Hrs/week (L)	**Type of Course:**	Practical
Examination Scheme	Oral 25 Marks		

Pre-requisites:Circuit building on breadboard

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	Oral Examination	External	25

Course Objectives

1	To Learn the process of inspecting a package ic using a microscope.
2	To Understand the content of a package bill of material meaning parts of the package
3	To build the ESP32 circuit on a breadboard.
4	To Study the Integrated circuit using a data sheet and compare with test parameters.

Course Outcomes: Students will be able to

614.1	Identify package parts required
614.2	Skilled in using the ESP32 package on a breadboard.
614.3	design a package leadframe.
614.4	Explain data sheet parameters and how they relate to the actual testing.
614.5	Gain skills to use CAD software design

List of experiments:

1) Optically and physical Inspect packaged IC structures
2) Understand types and steps of packaging in detail with physical parts involved in process
3) Draw flowchart, algorithm and write a code a small part of packaging sequence using ESP32 library in Arduino
4) To build the circuit of practical 3 on a breadboard to realize the output
5) Learn the functioning of FreeCAD software (FreeCAD)
6) To measure the dimensions of given packaged IC and build a lead frame for the same in FreeCAD software (FreeCAD)
7) To thoroughly study and understand provided IC Datasheet
8) To perform I-V characteristics of provided IC from practical 7 and match with datasheet

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Final Year Electronics and Telecommunications (2022 Course) Semiconductor Wafer Fabrication. ETHDT 707			
Course Code:	**ETHDT707**	**Credit**	3
Contact Hours:	3 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Examination: 40 Marks	End-sem. Examination: 60Marks	

Pre-requisites: Digital Logic Design,Basic programming skills

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-sem. Examination	Internal	40
2.	End Semester Examination	External	60

Course Objectives

1	Provide students overall understanding of the semiconductor fabrication process.
2	Demonstrate some of the operations through labs to clear the concepts.
3	Understand various types of fabrication processes and node types.
4	Appreciate the accuracy and precision needed during wafer fabrication.

Course Outcomes: Students will be able to

707.1	Understand various semiconductor materials, chemicals and gases used in wafer fabrication.
707.2	Learn how raw silicon wafers are produced.
707.3	Put the knowledge learned together to experiment on lithography using a simple mask.
707.4	Know how the wafers are sample tested, analyzed for failures and quality monitored.
707.5	Explain Quality and reliability matrix for fabrication

Topics covered:

UNIT I: Fabrication facility
Overview of different sections of fabrication facility, Chemicals and gasses needed, Environmental compliance, Safety protocols, process monitoring, process integration.
UNIT II: Semiconductor materials and initial process
Semiconductor materials, Semiconductor process types cmos, bipolar, Bicmos, RF, power, Making of silicon ingot and raw material, Wafer slicing, polishing and thickness control.
UNIT III: Wafer dice formation
Annealing, Oxidation and relevant machines, Photolithography, Etching, Ion implantation/Doping, Mask preparation from GDS file, Metallisation and its materials Passivation process, ET structure and its testing
UNIT IV:Types of fabrication processes
Bipolar process, nMOS process, CMOS process, how different fabrication lines differ from each other
UNIT V:Quality and Reliability
Quality and reliability matrix for fabrication, quality control gates and in process measurements, lot acceptance and rejection criterion, Failure analysis, Ongoing reliability monitoring.

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Text Books:

1. Microchip Fabrication: A Practical Guide to Semiconductor Processing, Sixth Edition. Peter Van Zant

Reference Books:

1. Integrated circuit Fabrication Technology: David J Elliot, McGraw-Hill Inc

E- Books / E- Learning References:

https://www.youtube.com/watch?v=DiFovfCtvgw

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Third Year Electronics and Telecommunications (2022 Course) Semiconductor Processing Lab ETHDT 708			
Course Code:	**ETHDT708**	**Credit**	**2**
Contact Hours:	4 Hrs/week (L)	**Type of Course:**	Practical
Examination Scheme	Oral-25 Marks Termwork-25Marks		

Pre-requisites:Measurement techniques

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	Oral Examination	External	25
2.	Term Work	Internal	25

Course Objectives

1	To prepare masks required for photolithography.
2	To understand the wet bench process to etch out in fabrication.
3	To develop understanding of lithography setup and process steps
4	To Characterize semiconductor material for doping, mobility and sheet resistance

Course Outcomes: Students will be able to

708.1	Design and make masks required for semiconductor photolithography
708.2	Perform setup of lithography and make use of it for wafer fabrication.
708.3	Etch a given pattern using a wet bench to form an active component structure.
708.4	Perform various measurements to characterize the given sample of semiconductor material.
708.5	Learn hall effects.

List of experiments:

1) Prepare an example lithography mask for fabrication of BJT.
2) Prepare an example lithography mask for fabrication of MOSFET.
3) To study the Chemical wet bench and Wafer cleaning.
4) Demonstrate basic cleaning procedure with all precautions
5) To understand the components of a simple photolithography system.
6) Create a simple photolithography system to further appreciate the process and its working principle.
7) Perform the photolithography procedure using the mask designed in practical 1.
8) Perform the photolithography procedure using the mask designed in practical 2
9) Characterize the fabricated specimen p+ by physical inspection and optical measurement.
10) Characterize the fabricated specimen n+ by physical inspection and optical measurement.
11) Etch the prepared specimen from practical 7 and conduct optical measurements.
12) Etch the prepared specimen from practical 8 and conduct optical measurements
13) To perform electron density measurements on semiconductor wafers.
14) To perform sheet resistance measurements on semiconductor wafers.
15) To understand the Van Der Pauw Hall measurement setup and measure mobility.
16) Study given TLM structures using hall effect.

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Final Year Electronics and Telecommunications (2022 Course) Semiconductor Integrated Circuit Design. ETHDT 803			
Course Code:	**ETHDT803**	**Credit**	**3**
Contact Hours:	3 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Examination: 40 Marks	End-sem. Examination: 60Marks	

Pre-requisites: Integrated circuit basics.

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-sem. Examination	Internal	40
2.	End Semester Examination	External	60

Course Objectives

1	Provide students with knowledge of high level IC design process flow
2	Provide examples of simple chip designs.
3	Demonstrate difference between logical design and physical design.
4	Explain the need for DFT and DFM in the ic design cycle.

Course Outcomes: Students will be able to

803.1	Understand the IC design process flow.
803.2	Differentiate between different types of IC designs.
803.3	Gain knowledge of IC design software.
803.4	Explain design and wafer foundry interaction.
803.5	Solve basic design challenges in semiconductor technology using learned concepts.

Topics covered:

UNIT I: Integrated Circuit (IC) Design process.

The design cycle, Design consideration, data sheet relevance, IC families, Transistor level design, Register transfer level design.

UNIT II:Digital design

Basics of digital design, spice modeling and simulation, MOS design, CMOS logic, timing and I/O, latches, flip flops and synchronous systems, bipolar and bi-cmos logic, memories, Gaas circuits.

UNIT III: Analog design

Integrated circuit devices and modeling, processing and layout, amplifiers, opamp, comparator, A/D and D/A converters, filters,Phase locked loops,RF design.

UNIT IV:IC design EDA/CAD tools

Examples of CAD softwares, software features, Hardware and license requirement for design software, IP usage and royalty, Scan chain, logic bist, memory bist, design for testability, design for manufacturability

UNIT V: IC design examples

Differences between Digital, Analog, Power and RF, Mixed signal design, System on Chip design examples, What happens after design is given to wafer foundry, Design revisions

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Text Books:

1.Analysis And Design Of Analog Integrated Circuits - Paul R. Gray And Meyer.
2.CMOS Analog Circuit Design - Phillip E. Allen.

Reference Books:

1. Design of Analog CMOS Integrated Circuits - Behzad Razavi.
2. Analog Integrated Circuit Design - Carusone, David A. Johns, and Kenneth W. Martin.

E- Books / E- Learning References:

https://www.youtube.com/watch?v=vDKzpKUvab4

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Final Year Electronics and Telecommunications (2022 Course) Intergrated Circuit Design Lab ETHDT 804			
Course Code:	**ETHDT708**	**Credit**	**2**
Contact Hours:	4 Hrs/week (L)	**Type of Course:**	Practical
Examination Scheme	Oral-25 Marks Termwork-25Marks		

Pre-requisites:Measurement techniques

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	Oral Examination	External	25
2.	Term Work	Internal	25

Course Objectives

1	To introduce EDA tools required for IC design.
2	To learn IP and core library creation.
3	To Understand PMOS/NMOS and inverter circuit design.
4	To learn the relation between design and wafer mask creation.

Course Outcomes: Students will be able to

804.1	Explain the flow of EDA tools for IC design.
804.2	Create design IP and libraries.
804.3	Design simple pms/nmos inverter circuit.
804.4	Observe changes between die and package measurements.
804.5	Compare die and package characteristics.

List of experiments:

1)To get introduced to Cadence IC Design EDA tools and get a hands on student version.
2) Learn Synopsys IC Design EDA tools and get a hands on student version.
3) Understand the Prerequisites for design and learn to create I/O libraries
4) Get to know Prerequisites for design and create standard cell libraries
5) PMOS structure design in the EDA software.
6) Designing a NMOS structure in the software.
7) Inverter design using the libraries designed in practical 5 &6.
8) Gate design using the libraries designed in practical 5 &6.
9) Static parameter analysis of the inverter designed in practical 7&8.
10) To execute dynamic parameter analysis of the inverter designed in practical 7&8.
11) Design mask structures for mask alignment based on learnt concepts.
12) Design masks for multiple layers based on learnt concepts.
13) To build IP use case from the designs created during the practicals
14) Simulate non-linear models for die and packaged ICs and observe the differences.
15) Learn steps to design a simple digital IC.
16) Learn steps to design a simple RF IC

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