AISSMS
INSTITUTE OF INFORMATION TECHNOLOGY
(IOIT)

ADDING VALUE TO ENGINEERING

An Autonomous Institute Affiliated to Savitribai Phule Pune University
Approved by AICTE, New Delhi and Recognised by Govt. of Maharashtra
Accredited by NAAC with "A+" Grade | NBA - 5 UG Programmes

ACADEMIC COURSE STRUCTURE
[as per NEP]

ELECTRONICS AND TELECOMMUNICATION ENGINEERING

M.TECH 2 YEAR PG COURSE
(Applicable for the batches admitted from 2023-2024)

AISSMS INSTITUTE OF INFORMATION TECHNOLOGY
Kennedy Road, Near RTO,
Pune – 411 001, Maharashtra State, India
Email: principal@aissmsioit.org, Website:
https://www.aissmsioit.org

Institute Vision & Mission

Vision

To be recognized amongst top 10 private engineering colleges in Maharashtra by the year 2026 byrendering value added education through academic excellence, research, entrepreneurial attitude, and global exposure.

Mission

- To enable placement of 150 plus students in the 7 lacs plus category &ensure 100% placement of all final year students
- To connect with 10 plus international universities, professional bodies and organizations to provide global exposure to students
- To create conducive environment for career growth, prosperity, and happiness of 100% staff.
- To be amongst top 5 private colleges in Pune in terms of admission cut off.

Quality Policy

We commit ourselves to provide quality education & enhance our students quality through continuous improvement in our teaching and learning processes.

Department Vision & Mission

Vision

To be one of the renowned Electronics & Telecommunication Engineering programmes imparting quality education by promoting professionalism, values, and ethics leading to a progressive career in industry & academia globally.

Mission

- To boost employability/entrepreneurship/higher studies through value-added activities.
- To inculcate research attitude and professional ethics for addressing the needs of industry.

Program Educational Objectives (PEOs)

Graduates will

1. Engage in solving problems in the E&TC domain by developing products/offering services to cater to the needs of the society.
2. Work in diverse career fields of information and communication technology.
3. Develop new methodologies and technologies for solving real-life problems

Program Outcomes (POs)

1. Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems. [Engineering knowledge]
2. Identify, formulate, research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences. [Problem analysis]
3. Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations. [Design/development of solutions]
4. Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions. [Conduct investigations of complex problems]
5. Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations. [Modern tool usage]
6. Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice. [The engineer and society]
7. Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development. [Environment and sustainability]
8. Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice. [Ethics]
9. Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings. [Individual and team work]
10. Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions. [Communication]
11. Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments. [Project management and finance]
12. Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change. [Life-long learning]

Program Specific Outcomes (PSOs)

Graduates will be able to

1. Apply domain-specific knowledge to analyze, design and develop electronics and telecommunication systems/applications in the field of Embedded Systems, Very Large Scale Integration (VLSI), Internet of Things (IoT), and Communication Technology.
2. Select and apply software and hardware tools such as Electronic Design Automation (EDA) and Test/Measurement equipment to solve engineering problems.

Program- Electronics and Telecommunication Engineering
M. Tech. (VLSI & Embedded Systems)
(Autonomous PG Structure)

A. Definition of Credit:

1 Hr. Lecture (L) per week	1 credit
1 Hr. Tutorial (T) per week	1 credit
1 Hr. Practical (P) per week 2 Hours Practical(Lab)/week	0.5 credits 1 credit

B. Range of credits –
A range of credits from 150 to 160 for a student to be eligible to get Post Graduate degree in Engineering.

C. Credit for Post Graduate Degree in Electronics and Telecommunication Engineering

Sr. No.	Year	Semester	Credits
1	First Year	I	**20**
2		II	**20**
3	Second Year	III	**20**
4		IV	**20**
	Total		**80**

D. Structure of Post Graduate Engineering program

Sr. No.	Domains	Code	Total Credits	As per NEP credits
1	Programme Core Courses	VLPCC	**29**	**44-56**
2	Professional Elective course	VLPEC	**06**	**20**
3	Vocational and Skill Engineering Course	VLVSE	**17**	**08**
4	Humanities Social Science and Management	VLHSM	**05**	**14**
5	Experimental Learning Courses	VLELC	**23**	**22**
Total Credits			**80**	**80-88**

E. Domain wise Credits Distribution:

Sr. No.	Domains	Code	Domain wise Credits Distribution					
			Semesters				Total Credits	As per NEP Credits
			I	II	III	IV		
1	Programme Core Courses	PCC	13	16	--	-	**29**	
2	Professional Elective Course	PEC	03	03	--	--	**08**	
3	Vocational and Skill Engineering Course	VSE	--	--	13	04	**17**	
4	Humanities Social Science and Management	HSM	01	01	03	--	**05**	
5	Experimental Learning Courses	ELC	03	--	04	16	**23**	
Total Credits			**20**	**20**	**20**	**20**	**80**	
Total Working Hours per Week			**22**	**22**	**36**	**36**	**-**	
Total Marks			**625**	**625**	**300**	**300**	**1850**	

F. Major Courses:

Sr. No.	Semester	Course Code	Course Title	Credits
1	Sem-I	VLPCC901	Digital CMOS Design	**04**
2	Sem-I	VLPCC902	Reconfigurable Computing	**03**
3	Sem-I	VLPCC903	Embedded System Design	**04**
4	Sem-I	VLPCC904	Lab Practice I	**02**
5	Sem-I	VLPEC905	Elective-I	**03**
6	Sem-II	VLPCC1001	Analog CMOS Design	**04**
7	Sem-II	VLPCC1002	System on Chip	**03**
8	Sem-II	VLPCC1003	Testing and Verification of VLSI Circuits	**04**
9	Sem-II	VLPCC1004	ASIC Design	**03**
10	Sem-II	VLPCC1005	Lab Practice II	**02**
11	Sem-II	VLPEC1006	Elective-II	**03**
			Total Major Courses Credits	**35**

G. Humanities Social Science and Management Courses:

Sr. No.	Semester	Course Code	Course Title	Credits
1	Sem-I	VLHSM907	Audit Course (Introduction to Constitution/Renewable Energy studies)	**01**
2	Sem-II	VLHSM1007	Audit Course (Human Values in Ethics and Education/Disaster Management)	**01**
3	Sem-III	VLHSM1102	Project and Finance Management	**03**
			Total Credits	**05**

H. Vocational and Skill Engineering Course

Sr. No.	Semester	Course Code	Course Title	Credits
1	Sem-III	VLVSE1101	Internship	**12**
2	Sem-III	VLVSE1103	Intellectual Property Rights	**01**
3	Sem-IV	VLVSE1201	Technical Paper Writing	**04**
			Total Credits	**17**

I. Experiential Learning Courses:

Sr. No.	Semester	Course Code	Course Title	Credits
1	Sem-I	VLELC906	Research Methodology	**03**
2	Sem-III	VLELC1103	Dissertation Stage I	**04**
3	Sem-IV	VCLELC1202	Dissertation Stage II	**16**
			Total Credits	**23**

J. Exit Course

Sr. No.	Course Title	Offered for class	Course Credits
1	Internship @	First Year M. Tech	06

@ Six week Internship to be completed by the students from VLSI and Embedded Systems Company along with certificate and detailed report.

M. Tech. (VLSI & Embedded Systems) - First Year (Semester – I)

Sr. No.	Code	Course Title	Hours per week			Credits	Examination scheme				
			L	T	P		Unit Test	End Sem	TW	OR/ Presentation	Total
1	VLPCC901	Digital CMOS Design	4	--	--	4	40#	60**	--	--	100
2	VLPCC902	Reconfigurable Computing	3	--	--	3	40#	60*	--	--	100
3	VLPCC903	Embedded System Design	4	--	--	4	40#	60**	--	--	100
4	VLPCC904	Lab Practice I	--	--	4	2	--	--	50	50	100
5	VLPEC905	Elective I	3	--	--	3	40#	60*	--	--	100
6	VLELC906	Research Methodology	3	--	--	3	40#	60*	--	--	100
7	VLHSM907	Audit Course (Introduction to Constitution/Renewable Energy studies)	1	--	--	01	--	--	25	--	25
		Total	**18**	--	**4**	**20**	**200**	**300**	**75**	**50**	**625**

L-Lecture, T-Tutorial, P-Practical

Elective I

Real Time Operating Systems	MOS Device Modeling and Characterization.
Embedded Product Design	Embedded Automotive Systems

* **End Semester Examination (ESE)** based on subjective questions.

** **Practical or Activity based Evolution.**

\# **In semester Activity based Evaluation** based on Presentation/Group Discussion/Laboratory Work/Course Project/Home Assignment/Comprehensive Viva Voce/Blog Writing/Case Study/Survey/Multiple-Choice Question (MCQ) examination.

M. Tech. (VLSI & Embedded Systems) - First Year (Semester – II)											
Sr. No.	**Code**	**Course Title**	**Hours per week**			**Credits**	**Examination scheme**				
			L	**T**	**P**		**Unit Test**	**End Sem**	**TW**	**OR/ Presentation**	**Total**
1	VLPCC1001	Analog CMOS Design	4	--	--	4	40#	60**	--	--	100
2	VLPCC1002	System on Chip	3	--	--	3	40#	60*	--	--	100
3	VLPCC1003	Testing and Verification of VLSI Circuits	4	--	--	4	40#	60**	--	--	100
4	VLPCC1004	ASIC Design	3	--	--	3	40#	60*	--	--	100
5	VLPCC1005	Lab Practice II	--	--	4	2	--	--	50	50	100
6	VLPEC1006	Elective II	3	--	--	3	40#	60*	--	--	100
7	VLHSM 1007	Audit Course (Human Values in Ethics and Education/Disaster Management)	1	--	--	1	--	--	25	--	25
		Total	**18**	--	**4**	**20**	**200**	**300**	**75**	**50**	**625**

L-Lecture, T-Tutorial, P-Practical

Elective II	
Mixed Signal IC Design	High Speed ICs
VLSI Signal Processing	

* **End Semester Examination (ESE)** based on subjective questions.

** **Practical or Activity based Evolution.**

In semester Activity based Evaluation based on Presentation/Group Discussion/Laboratory Work/Course Project/Home Assignment/Comprehensive Viva Voce/Blog Writing/Case Study/Survey/Multiple-Choice Question (MCQ) examination.

M. Tech. (VLSI & Embedded Systems) – Second Year (Semester–III)											
Sr. No.	**Code**	**Course Title**	**Hours per week**			**Credits**	**Examination scheme**				
			L	**T**	**P**		**Unit Test**	**End Sem**	**TW**	**OR/ Presentation**	**Total**
1	VLVSE1101	Internship	--	--	24	12	--	--	100	--	**100**
2	VLHSM1102	Project and Finance Management	3	--	--	03	--	--	50	--	**50**
3	VLVSE1103	Intellectual Property Rights	1	--	--	01	--	--	50	--	**50**
4	VLELC1104	Dissertation Stage I	--	--	8	04	--	--	50	50	**100**
		Total	**04**	--	**32**	**20**	**50**	**50**	**250**	**50**	**300**

L-Lecture, T-Tutorial, P-Practical

M. Tech. (VLSI & Embedded Systems) – Second Year (Semester –IV)											
Sr. No.	**Code**	**Course Title**	**Hours per week**			**Credits**	**Examination scheme**				
			L	**T**	**P**		**Unit Test**	**End Sem**	**TW**	**OR/ Presentation**	**Total**
1	VLVSE1201	Technical Paper Writing	--	04	--	04	--	--	50	50	**100**
2	VLELC1202	Dissertation Stage II	--	--	32	16	--	--	150	50	**200**
		Total	--	**04**	**20**	**20**	--	--	**200**	**100**	**300**

L-Lecture, T-Tutorial, P-Practical

M. Tech First Year Electronics and Telecommunications (2023 Course) Digital CMOS Design			
Course Code:	**VLPCC901**	**Credit**	**4**
Contact Hours:	4 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Evaluation 40 Marks	End-sem. Examination (Activity based) 60 Marks	

Pre-requisites:

- MOSFET, Digital Circuits, CMOS design

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-Sem. Evaluation	Internal	40
2.	End Semester Examination (Activity based)	External	60

Course Objectives	
1	To learn MOSFET Models and layout fundamentals
2	To nurture students understanding in performance parameters of digital CMOS Design
3	To understand the advanced trends in CMOS design
4	To learn the delay models

Course Outcomes: Students will be able to	
901.1	Understand the fundamentals of CMOS Technology in Digital Domain
901.2	Explore the skills of designing digital VLSI
901.3	Demonstrate the ability of using EDA tools in IC Design

Topics covered:

Module I: MOSFET Models and Layout (10 hrs.)

MOS Capacitance models, MOS Gate Capacitance Model, MOS Diffusion Capacitance Model. Non ideal I-V Effects, MOSFET equivalent circuits and analysis, Parasitic; Technology scaling; Lambda parameter; wiring parasitic; SPICE Models, CMOS layout techniques; Transient response. CMOS Technologies: Layout Design Rules CMOS Process Enhancements: Transistors, Interconnect, Circuit Elements, Beyond Conventional CMOS. CMOS Fabrication and Layout: Inverter Cross-section, Fabrication Process, Stick Diagrams..

Module II: Performance parameters (10 hrs.)

Static, dynamic and short circuit power dissipations, Propagation delay, Power delay product, Fan in, fan out and dependencies. Delay Estimation**:** RC Delay Models, Linear Delay Model, Logical Effort, Parasitic Delay. Logical Effort and Transistor Sizing: Delay in a Logic Gate, Delay in Multistage Logic Networks, Interconnect: Resistance, Capacitance, Delay, Crosstalk. Design Margin.

Module III: Logic design (10 hrs.) Static CMOS Logic : Inverter, NAND Gate, Combinational Logic, NOR Gate, Compound Gates, Pass Transistors and Transmission Gates, Tristates, Multiplexers, Latches and Flip- Flops, Design calculations for combinational logic and active area on chip; Hazards, sources and mitigation techniques, case study; HDL codes for FSM, Meta-stability and solutions; Transmission gate, utility and limitations.
Module IV: Advanced trends (10 hrs.) Circuit Families: Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Domino logic, NORA logic, Differential Circuits, Sense Amplifier Circuits, BiCMOS Circuits, Low Power Logic Design, Comparison of Circuit Families, Materials for performance improvement, Techniques for Low power, High speed designs.

Text Books:

1. Neil Weste and Kamaran, "Principles of CMOS VLSI Design", Education Asia.
2. M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits: A Design Perspective, Pearson (Low Price Edition).

Reference Books:

1. S-M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits : Analysis and Design, Third Edition, McGraw-Hill
2. Charls Roth, "Digital System Design using VHDL", Tata McGraw Hill.
3. Samir Palnitkar, "Verilog HDL – A Guide to Digital Design and Synthesis", PHI

M. Tech First Year Electronics and Telecommunications (2023 Course)
Reconfigurable Computing

Course Code:	**VLPCC902**	**Credit**	**3**
Contact Hours:	3 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Evaluation 40 Marks	End-sem. Examination 60 Marks	

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-Sem. Evaluation	Internal	40
2.	End Semester Examination	External	60

Course Objectives

1	To understand various computing architectures
2	To provide students the concept of handling issues of reconfigure computing
3	To provide students implementation approaches of FPGA design in view of reconfiguration
4	To outline various applications reconfigure computing

Course Outcomes: Students will be able to

902.1	Understand the concept of reconfigurable computing and its integration on computing platforms.
902.2	Design, implement and analyze reconfigurable systems in the recent application domains using HDL.
902.3	Use advanced EDA tools to simulate and synthesize HDL codes for reconfigurable architectures.

Topics covered:

Module I: (9 hrs.)
Domain of RC: General Purpose Computing, Domain-Specific Processors, Application-Specific Processors, Reconfigurable Computing, Fields of Application. Architecture of Field Programmable Gate Arrays, Reconfigurable Processing Fabric (RPF) Architectures: Fine grained, Coarse-Grained, Integration of RPF into Traditional Computing Systems.

Module II: (9 hrs.)
Early systems of Reconfigurable computing: PAM, VCC, Splash, PRISM, Teramac, Cray, SRC, non-FPGA research, other issues; Reconfiguration Management: Reconfiguration, Configuration architectures, managing reconfiguration process, reducing reconfiguration time, configuration security.

Module III: (9 hrs.)
Implementation: Integration, FPGA Design Flow, System On A Programmable Chip: Introduction to SoPC, Adaptive Multiprocessing on Chip. Reconfiguration Project Design Approaches: J-Bit, Modular, Early Access, Vivado.

Module IV: (9 hrs.)
RC Applications: Implementing applications with FPGAs, various applications and use of reconfiguration: Video Streaming, , Distributed arithmetic, Adaptive Controller, Adaptive cryptographic systems, Software Defined Radio, High-Performance Computing, Automatic target recognition systems.

Text Books:

1. Bobda Christophe, "Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications", Springer.
2. Hauck Scott, Dehon A, "Reconfigurable Computing: The Theory and Practice of FPGA- Based Computation", Elsevier.

Reference Books:

1. Vivado Partial Reconfiguration.pdf: user guide 909 by Xilinx Revision: 04/06/2016.

M. Tech First Year Electronics and Telecommunications (2023 Course) Embedded System Design			
Course Code:	**VLPCC903**	**Credit**	**44**
Contact Hours:	4 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Evaluation 40 Marks	End-sem. Examination (Activity based) 60 Marks	

Pre-requisites:

- MOSFET, Digital Circuits, CMOS design

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-Sem. Evaluation	Internal	40
2.	End Semester Examination (Activity based)	External	60

Course Objectives	
1	To understand various design issues in embedded systems
2	To learn ARM 9 architecture and its programming concepts
3	To learn embedded LINUX operating system
4	To make aware of the significance of embedded network processors

Course Outcomes: Students will be able to	
903.1	Design ARM Processor based Embedded Systems
903.2	Carry out programming in Embedded programming in C, C++
903.3	Port Linux operating system and device drivers
903.4	Understand attributes of functional units of Network Protocol

Topics covered:

Module I: (10 hrs.)

Introduction to Embedded Systems: Introduction to Embedded Systems, Architecture of Embedded System, Design Methodology, Design Metrics, General Purpose Processor, System On chip. Embedded system design and development **:** Embedded system design, Life-Cycle Models, Development tools, Introduction to Development Platform Trends (only introduce IDE, board Details and Application) Arduino, Beaglebone, Rasberry PI, Intel Galileo Gen 2 .

Module II: (10 hrs.) ARM CORTEX series features; Improvement over classical series, CORTEX ARM processors series, Features and applications, Survey of CORTEX based controllers from various manufacturers, ARM-M3 Based Microcontroller LPC1768: Features, Architecture block diagram & its description, System Control, Clock & Power Control, Pin Connect Block. CMSIS Standard, Bus Protocols Ethernet, CAN, USB, Bluetooth.
Module III: (10 hrs.) Embedded Linux: System architecture, BIOS versus boot-loader, Booting the kernel, Kernel initialization, Space initialization, Boot loaders and Storage considerations. Linux kernel construction: Kernel build system, Obtaining a custom Linux kernel, File systems, Device drivers, Kernel configuration.
Module IV: (10 hrs.) Embedded System Design Case Studies: Design Case Studies like Automated Meter Reading Systems (AMR), Digital Camera, Certification and documentation: Mechanical Packaging, Testing, reliability and failure analysis, Certification (EMI / RFI) and Documentation. Study of any two real life embedded products in detail.

Text Books:

1. Noergaard Tammy, "Embedded Systems Architecture", Elsevier Publication.
2. Hallinan Christopher, "Embedded Linux Primer: A Practical Real-World Approach", Second Edition, Pearson Education.
3. Shibu,"Introduction to Embedded Systems", TMH.
4. Comer D E, "Network System Design using Network Process", PHI

Reference Books:

1. www.nxp.com/documents/user_manual/UM10360.pdf.
2. Croeley Patrick, Franklin M. A, Hadimioglu H & Onufryk P Z, "Network Processor Design, Issues and Practices", vol-1-2, Elsevier.
3. Uyless Black, "Computer Networks-Protocols, Standards Interfaces", Second Edition, PHI.
4. http://www.npforum.org/;http://www.intel.com/design/network/products/npfamily.

M. Tech First Year Electronics and Telecommunications (2023 Course)
Research Methodology

Course Code:	**VLELC906**	**Credit**	**3**
Contact Hours:	3 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Evaluation 40 Marks	End-sem. Examination 60 Marks	

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-Sem. Evaluation	Internal	40
2.	End Semester Examination	External	60

Course Objectives

1	To learn the process of identification of research problem
2	To understand the importance of statistics involved in research
3	To understand the process of analysis and verification of developed system model
4	To develop a skill to prepare research proposals

Course Outcomes: Students will be able to

906.1	Outline research problem, its scope, objectives and errors
906.2	Understand basic instrumentation schemes and its data collection methods
906.3	Learn various statistical techniques
906.4	Develop model and can predict the performance of experimental system
906.5	Write research proposals of their own domain

Topics covered:

Module I: (9 hrs.)

Research Problem: Meaning of research problem, Sources of research problem, Criteria/ Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Basic instrumentation: Instrumentation schemes, Static and dynamic characteristics of instruments used in experimental set up, Performance under flow or motion conditions, Data collection using a digital computer system, Linear scaling for receiver and fidelity of instrument, Role of DSP is collected data contains noise.

Module II: (9 hrs.)

Applied Statistics: Regression analysis, Parameter estimation, Multivariate statistics, Principal component analysis, Moments and response curve methods, State vector machines and uncertainty analysis.

Module III: (9 hrs.)
Modelling and prediction of performance: Setting up a computing model to predict performance of experimental system, Multi-scale modeling and verifying performance of process system, Nonlinear analysis of system and asymptotic analysis, Verifying if assumptions hold true for a given apparatus setup, Plotting family of performance curves to study trends and tendencies, Sensitivity theory and applications.

Module IV: (9 hrs.)
Developing a Research Proposal: Format of research proposal, Individual research proposal, and Institutional proposal. Proposal of a student – a presentation and assessment by a review committee consisting of guide and external expert only. Other faculty members may attend and give suggestions relevant to topic of research.

Text Books:

1. Dr. Kothari C R, "Research Methodology: Methods and Trends".
2. Ranjit Kumar, "Research Methodology: A Step by Step Guide for Beginners", Second edition.

Reference Books:

1. Melville Stuart, Goddard Wayne, "Research methodology: An Introduction for Science & Engineering students".
2. Dr. Sharma S D, Kedar Nath, "Operational Research".

M. Tech First Year Electronics and Telecommunications (2023 Course)
Real Time Operating Systems (Elective I)

Course Code:	**VLPEC905**	**Credit**	**4**
Contact Hours:	4 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Evaluation 40 Marks	End-sem. Examination 60 Marks	

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-Sem. Evaluation	Internal	40
2.	End Semester Examination	External	60

Course Objectives

1	To understand software Architecture and Development cycle of Operating Systems
2	To learn various management attributes of Operating System
3	To understand RTOS
4	To study Linux/ RT Linux environment

Course Outcomes: Students will be able to

905.1	List Embedded Software Developments Tools
905.2	Learn Software Development Process Life Cycle
905.3	Gain knowledge of Real Time Operating Systems with respect to uCOS
905.4	Understand RT Linux operating System

Topics covered:

Module I: (10 hrs.)
Software Architectures, Software Developments Tools, Programming Concepts, Embedded Programming in C and C++, Queues, Stacks, Optimization of Memory needs, Program Modeling Concepts, Software Development Process Life Cycle and its Model, Software Analysis, Design and Maintenance

Module II: (10 hrs.)
Operating System Concepts, Processes, Deadlocks, Memory Management, Input /Output, Files, Security, the Shell, Recycling of Concepts. Operating system structure Monolithic Systems: Layered Systems, Virtual Machines, Exo-kernels, Client-Server Model

Module III: (10 hrs.)
Real Time Operating Systems (µC/OS):Real-Time Software Concepts, Kernel Structure, Task Management, Time Management, Inter task Communication & Synchronization, Memory Management, and Porting µCos-II.

Module IV: (10 hrs.)
Linux/RT Linux: Features of Linux, Linux commands, File Manipulations, Directory, Pipes and Filters, File Protections, Shell Programming, System Programming, RT Linux Modules, POSIX Threads, Mutex Management, Semaphore Management.

Text Books:

1. Labrossy J. J, Lawrence, "µC/OS-II, The real time Kernel", R & D Publication.
2. Dr Prasad K V K K, "Embedded Real Time Systems: Concepts, Design & Programming", Dreamtech Publication**.**
3. Simon D. E, "An Embedded Software Primer", Pearson education.

Reference Books:

1. Tanenbaum A S, "Modern Operating Systems", Prentice Hall.
2. Raj Kamal, "Embedded Systems Architecture, Programming and design", Tata McGraw-Hill

M. Tech First Year Electronics and Telecommunications (2023 Course)
MOS Device Modeling and Characterization (Elective I)

Course Code:	**VLPEC905**	**Credit**	**3**
Contact Hours:	3 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Evaluation 40 Marks	End-sem. Examination 60 Marks	

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-Sem. Evaluation	Internal	40
2.	End Semester Examination	External	60

Course Objectives

1	To provide detail understanding of MOS devices' structures and operations
2	To understand the effect of various materials on the characteristics of MOSFET
3	To acquaint the students with SPICE tool for modeling of transistor behavior
4	To provide a brief knowledge of Advanced MOSFET models

Course Outcomes: Students will be able to

905.1	Analyze MOSFET models
905.2	Learn MOSFET characterization using SPICE simulation
905.3	Gain information about advanced MOSFET models
905.4	Understand non-classical MOS structures

Topics covered:

Module I: (10 hrs.)
A qualitative Description of MOS Transistor operation, contact potentials, two terminal MOS structure: Flat band voltage, Potential balance and charge balance, Effect of Gate-Substrate voltage on Surface Condition, Inversion, Small signal capacitance.

Module II: (10 hrs.)
Short channel MOSFET, Small Dimension Effects, Channel length Modulation, Barrier lowing two dimensional charge sharing and threshold voltage, Punch through, Carrier velocity Saturation, Hot carrier Effects, Scaling, Effects due to thin oxides and high doping, mobility degradation.

Module III: (10 hrs.)
Modeling of Transistor using SPICE: Basic concepts, The level 1 Equations, The Level 2 Equations, The Level 3 Equations, Comparison of SPICE Models, Capacitance Models, Basic MOSFET models, Comparison of MOSFET Models.

Module IV: (10 hrs.)
Advanced MOSFET models for circuit simulators, Surface potential models, inversion charge based models, Compact MOSFET models, threshold voltage based model models, advanced MOSFET structures such as FINFET.

Text Books:

1. YannisTsividis, "Operation and modeling of the MOS transistor", Oxford University Press.
2. Kang S. M , "CMOS Digital Integrated Circuits", Tata Mc-Graw Hill.
3. Carlos Galup&Montoro, "MOSFET Modeling for Circuit Analysis and Design", World Scientific.
4. Donald Neamen, "Semiconductors Physics and Devices", Tata Mc-Graw Hill.

Reference Books:

1. Sze S. M, "Physics of Semiconductor Devices, Second Edition, Wiley Publications

M. Tech First Year Electronics and Telecommunications (2023 Course)
Embedded Product Design (Elective I)

Course Code:	**VLPEC905**	**Credit**	**3**
Contact Hours:	3 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Evaluation 40 Marks	End-sem. Examination 60 Marks	

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-Sem. Evaluation	Internal	40
2.	End Semester Examination	External	60

Course Objectives

1	To understand design challenges of embedded hardware and software
2	To gain knowledge of testing and verification issues in design cycle
3	To introduce h/w and s/w design models with different technology
4	To learn the importance of documentation for technology transfer

Course Outcomes: Students will be able to

905.1	Learn specifications and design challenges of embedded products
905.2	Estimate cost of embedded product
905.3	Understand the aspects of Mechanical Packaging, Testing, reliability and failure analysis, EMI/RFI Certification and Documentation
905.4	Demonstrate the knowledge of embedded product design related hardware and software design tools

Topics covered:

Module I: (9 hrs.)
Overview of Embedded Products: Need, Design challenges, product survey, specifications of product need of hardware and software, Partitioning of the design into its software and hardware components, Iteration and refinement of the partitioning.

Module II: (9 hrs.)
Deign Models and Techniques: various models of development of hardware and software, their features, different Processor technology, IC technology, Design Technology.

Module III: (9 hrs.)
Modules of Hardware and Software: Tradeoffs, Custom Single-purpose processors, General purpose processors, Software, Memory, Interfacing, Design technology-Hardware design, FPGA design, firmware design, driver development, RTOS porting, cost reduction, reengineering, optimization, maintenance, validation and development, prototyping, turnkey product design.

Module IV: (9 hrs.)
Testing and verification: Embedded products-areas of technology, Design and verification, Integration of the hardware and software components, testing- different tools, their selection criterion. Certification and documentation: Mechanical Packaging, Testing, reliability and failure analysis, communication protocols, Certification (EMI/ RFI) and its documentation. Study of any two real life embedded products in detail.

Text Books:

1. Vahid Frank and Tony Givargis , “Embedded System Design: A Unified Hardware/Software Introduction”, John Wiley Publication.

Reference Books:

1. Marwedel P, “Embedded System Design”, Springer Publication

M. Tech First Year Electronics and Telecommunications (2023 Course)
MOS Device Modeling and Characterization (Elective I)

Course Code:	**VLPEC905**	**Credit**	**3**
Contact Hours:	3 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Evaluation 40 Marks	End-sem. Examination 60 Marks	

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-Sem. Evaluation	Internal	40
2.	End Semester Examination	External	60

Course Objectives

1	To provide detail understanding of MOS devices' structures and operations
2	To understand the effect of various materials on the characteristics of MOSFET
3	To acquaint the students with SPICE tool for modeling of transistor behavior
4	To provide a brief knowledge of Advanced MOSFET models

Course Outcomes: Students will be able to

905.1	Analyze MOSFET models
905.2	Learn MOSFET characterization using SPICE simulation
905.3	Gain information about advanced MOSFET models
905.4	Understand non-classical MOS structures

Topics covered:

Module I: (10 hrs.)
A qualitative Description of MOS Transistor operation, contact potentials, two terminal MOS structure: Flat band voltage, Potential balance and charge balance, Effect of Gate-Substrate voltage on Surface Condition, Inversion, Small signal capacitance.

Module II: (10 hrs.)
Short channel MOSFET, Small Dimension Effects, Channel length Modulation, Barrier lowing two dimensional charge sharing and threshold voltage, Punch through, Carrier velocity Saturation, Hot carrier Effects, Scaling, Effects due to thin oxides and high doping, mobility degradation.

Module III: (10 hrs.)
Modeling of Transistor using SPICE: Basic concepts, The level 1 Equations, The Level 2 Equations, The Level 3 Equations, Comparison of SPICE Models, Capacitance Models, Basic MOSFET models, Comparison of MOSFET Models.

Module IV: (10 hrs.)
Advanced MOSFET models for circuit simulators, Surface potential models, inversion charge based models, Compact MOSFET models, threshold voltage based model models, advanced MOSFET structures such as FINFET.

Text Books:

1. YannisTsividis, "Operation and modeling of the MOS transistor", Oxford University Press.
2. Kang S. M , "CMOS Digital Integrated Circuits", Tata Mc-Graw Hill.
3. Carlos Galup&Montoro, "MOSFET Modeling for Circuit Analysis and Design", World Scientific.
4. Donald Neamen, "Semiconductors Physics and Devices", Tata Mc-Graw Hill.

Reference Books:

1. Sze S. M, "Physics of Semiconductor Devices, Second Edition, Wiley Publications

M. Tech First Year Electronics and Telecommunications (2023 Course) Lab Practice I			
Course Code:	**VLPCC904**	**Credit**	**2**
Contact Hours:	4 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	TW 50 Marks	OR 50 Marks	

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	Term Work	Internal	50
2.	Oral	External	50

The laboratory work will be based on completion of minimum two assignments/experiments confined to the courses of 1st semester of each subject. (**Laboratory Assignments/Experiments**)

Subject: DCD

1. To design, prepare layout and simulate CMOS Inverter for the given specifications of load capacitance, propagation delay, power dissipation, foundry etc.
2. To design logic for ATM machine password and access functionality. Assume suitable I/Os such as card sense, 4 digit PIN number, type of account, amount, other facilities needed etc.
3. To design CMOS logic for F = A + B (C + D) + EFG and prepare layout. Assume suitable capacitive load & foundry. Measure TR, TF& TPD.
4. To draw FSM diagram, write HDL code, synthesis, simulate, place & route for Tea/Coffee vending machine. Generalized I/Os of the machine are coin sense, cup sense, option sense, pour valve, timer count, alarm etc. You may assume additional I/Os too.
5. To design and simulate combinational logic to demonstrate hazards. Also, simulate the same logic redesigned for removal of hazards.

Subject: RC

1. To design and implement a Multi Context (4) 4-LUT and implement using HDL and download on FPGA.
2. Top level modular and hierarchical designs of Adder and Subtractor such that they can be replaced.
3. To design and implement a Multi Context (4) 4-LUT and implement using HDL and download on FPGA.
4. Top level modular and hierarchical designs of Adder and Subtractor such that they can be replaced.
5. An adaptive design of LED shifter (Right & Left shift)
6. SoPC based Hw-SW design (Soft/Hard Processor + FPGA HW

Subject: ESD

1. Write a program for 4*4 Matrix Keypad Interface.
2. To develop character device driver for GPIO
3. One experiment based on any one of development Platform: Arduino, Beaglebon, Rasberry Pi, Intel Galileo Gen 2.
4. Interfacing USB & CAN of LPC 1768.
5. Write a program for External Interrupt.

Subject: RM

1. Design a typical research problem using scientific method.
2. Design a data collection system using digital computer system.
3. Study the various analysis techniques.
4. Design and develop a computing model to predict the performance of experimental system.
5. Develop the following research proposal :A. Individual B. Institutional.

Subject: EPD

1. To estimate techno-commercial feasibility of any one embedded product such as mobile phone, programmable calculator, tablet PC, biometrics system, set top box etc.
2. To study design considerations of any one embedded product e.g. laptop, video conferencing system, surveillance/ security system, EMG/ECG machine etc.
3. To design any one embedded product to solve any real life problems.
4. To test the hardware designed for above assignment (3) using suitable simulation tool.
5. To simulate the software designed for the above assignment (3) using suitable simulation tool.

M. Tech First Year Electronics and Telecommunications (2023 Course) INTRODUCTION TO CONSTITUTION			
Course Code:	**VLHSM907**	**Credit**	**1**
Contact Hours:	1 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	TW 25		

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	Term Work	Internal	25

Course Objectives	
1	To acquaint students about their fundamental rights.
2	To inculcate directive principles basically "Fundamental Principles in governance of the country.
Course Outcomes: Students will be able to	
907.1	To introduce the students the philosophy of constitution of India.
907.2	To acquaint the students with their freedom and responsibilities.

Topics covered:

Module I: PHILOSOPHY OF THE INDIAN CONSTITUTION **(5 hrs.)**

a) Constitutional History of India
b) Role of Dr. B.R. Ambedkar in Constituent Assembly
c) Preamble - Source and Objects
d) Sovereign and Republic
e) Socialist and Secular
f) Democratic - Social and Economic Democracy
g) Justice - Social, Economic and Political
h) Liberty - Thought, Expression, Belief, Faith and Worship
i) Equality - Status and Opportunity
j) Fraternity, Human Dignity, Unity and Integrity of the Nation

Module II: FUNDAMENTAL RIGHTS **(10 hrs.)**

a) Right to equality
b) Right to freedoms
c) Right against exploitation
d) Right to freedom of religion
e) Cultural and educational rights
f) Right to property
g) Right to constitutional remedies

Module III: DIRECTIVE PRINCIPLES OF STATE POLICY **(10 hrs.)**

a) Equal Justice and free legal aid
b) Right to work and provisions for just and humane conditions of work
c) Provision for early childhood, Right to education and SC,ST, weaker section
d) Unifonn Civil Code
e) Standard of Living, nutrition and public health

f) Protection and improvement of environment
g) Separation of Judiciary from executive
h) Promotion of International peace and security

Module IV: FUNDAMENTAL DUTIES **(5 hrs.)**

a) Duty to abide by the Constitution
b) Duty to cherish and follow the noble ideals
c) Duty· to defend the country and render national service
d) Duty to value and preserve the rich heritage of our composite culture
e) Duty to develop scientific temper, humanism ,the spirit of inquiry & reform
f) Duty to safeguard public prope1ty and abjure violence
g) Duty to strive towards excellence

Text Books:

1. D. D. Basu, Introduction to the Constitution of India, LexisNexis
2. Granville Austin, The Constitution of India: Cornerstone of a Nation, Oxford University Press
3. Subhash Kashyap, Our Constitution, National Book Trust
4. M.P. Jain, Indian Constitutional Law, LexisNexis
5. V.N.Slmkla, Constitution of lndia, Eastern Book Company
6. P.M. Bakshi, The Constitution of India, Universal Law Publishing
7. M.V.Pylee, Constitutional Government in India, S. Chand
8. V. S. Khare, Dr. B.R.Ambedkar and India's National Security
9. डॉ. सत्यरंजन साठे, भारताच्या राज्यघटनेची ५० वर्षे, कॉन्टिनेन्टल प्रकाशन
10. नरेन्द्र चपळगावकर, राज्यघटनेचे अर्धशतक, मौज प्रकाशन गृह
11. सुहास पळशीकर, राजकारणाचा ताळेबंद भारतीय लोकशाहीची वाटचाल, साधना प्रकाशन
12. जयदेव गायकवाड, संविधान सभेत डॉ. आंबेडकर, पद्मगंगा प्रकाशन
13. झिया मोदी, टेन जजमेंट्स दॅट चेंज्ड् इंडिया, सकाळ प्रकाशन
14. डॉ. रावसाहेब कसबे, डॉ. आंबेडकर आणि भारतीय राज्यघटना, सुगावा प्रकाशन

M. Tech First Year Electronics and Telecommunications (2023 Course) RENUABLE ENERGY STUDIES			
Course Code:	**VLHSM907**	**Credit**	**1**
Contact Hours:	1 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	TW 25		

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	Term Work	Internal	25

Course Objectives	
1	To acquaint students about various energy studies
2	To inculcate students about uses of available energy sources for development of country.
Course Outcomes: Students will be able to	
907.1	To introduce the students various energy sources available.
907.2	To acquaint the students with natural sources of energy for multiple uses for nation growth.

Topics covered:

Module I: SOLOR ENERGY **(8 hrs.)**

Photovoltaic Systems: Introduction to the Major Photovoltaic System Types, Current– Voltage Curves for Loads, Grid-Connected Systems: Interfacing with the Utility, DC and AC Rated Power, The "Peak-Hours" Approach to Estimating PV Performance, Capacity Factors for PV Grid Connected Systems, PV Powered Water Pumping, PV systems – off grid systems and scope for inclusive growth of rural India.

Module II: WIND ENERGY **(8 hrs.)**

Wind Energy: wind speed and power relation, power extracted from wind, wind distribution and wind speed predictions. Wind power systems: system components, Types of Turbine, Choice of generators, electrical load matching, power control, Effect of wind speed variations, tower height and its effect, Variable speed operation, maximum power operation, control systems, Design consideration of wind farms and control

Module III: OTHER ENERGY SOURCES **(8 hrs.)**

Biomass – various resources, energy contents, technological advancements, conversion of biomass in other form of energy – solid, liquid and gases. Gasifiers, Biomass fired boilers, Co-firing, Generation from municipal solid waste, Issues in harnessing these sources. Mini and micro hydel plants scheme layout economics. Tidal and wave energy, Geothermal and Ocean-thermal energy conversion (OTEC) systems – schemes, feasibility and viability. Fuel cell- types and operating characteristics, efficiency, energy output of fuel cell.

Text Books:

1. 1. Renewable energy technologies - R. Ramesh, Narosa Publication.
2. 2. Energy Technology – S. Rao, Parulkar
3. 3. Non-conventional Energy Systems – Mittal, Wheelers Publication.
4. 4. Clark W. Gellings, "The Smart Grid: Enabling Energy Efficiency and Demand
5. Response", CRC Press
6. 5. Renewable Energy Technologies – Chetan Singh Solanki, PHI Learning Pvt. Ltd.

M. Tech First Year Electronics and Telecommunications (2023 Course)
Analog CMOS Design

Course Code:	**VLPCC1001**	**Credit**	**4**
Contact Hours:	4 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Evaluation 40 Marks	End-sem. Examination Activity based 60 Marks	

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-Sem. Evaluation	Internal	40
2.	End Semester Examination (Activity based)	External	60

Course Objectives

1	To understand theory of analog circuits using MOS small signal models
2	To understand design principles and techniques of CMOS Amplifiers
3	To gain design aspects of HF and Low Noise Amplifiers
4	To learn different methods of Stability and Frequency Compensation

Course Outcomes: Students will be able to

1001.1	Understand design concepts and issues of CMOS amplifiers
1001.2	Learn different Compensation techniques
1001.3	Acquire the knowledge of designing of HF and Low Noise Amplifiers

Topics covered:

Module I: (10 hrs.)
Current sources and References : MOSFET as switch, diode and active resistor; MOS Small-signal Models, Common Source Amplifier, The CMOS Inverter as an Amplifier, Weak inversion; Short channel regime; Current sinks and sources; Current mirrors; Current and voltage references, band gap reference.

Module II: (10 hrs.)
CMOS Amplifiers: Design of CMOS amplifiers, Inverting amplifiers, Cascode amplifiers, Differential amplifiers, Folded cascade; Current amplifiers, Output amplifier. Op Amps, high speed Op Amps, micro power Op Amps, low noise Op Amps.

Module III: (10 hrs.)
Comparators, Stability and Frequency Compensation: General considerations, Multi-pole systems, Phase Margin, Frequency Compensation, Compensation of two stage Op Amps, Slewing in two stage Op Amps and Other compensation techniques.

Module IV: (10 hrs.)
HF Amplifiers &Low Noise Amplifier: Open and Short circuit methods to estimate bandwidth, multistage amplifier for high bandwidth, Low Noise Amplifier (LNA) design, noise and power trade off, optimizations, Design of mixer, Advanced trends in Radio Frequency (RF) chip design.

Text Books:

1. Razavi B,"Design of Analog CMOS Integrated Circuits", McGraw-Hill.
2. Thomas Lee, "The Design of CMOS Radio – Frequency Integrated Circuits", Second edition, Cambridge.

Reference Books:

1. Allen P E and Holberg D R, CMOS Analog Circuit Design, Second Edition, Oxford University Press.
2. Gray P, Hurst P. J, Lewis S. H and Meyer R, "Analysis and Design of Analog Integrated Circuits", Fourth edition, Wiley.

M. Tech First Year Electronics and Telecommunications (2023 Course) System on Chip			
Course Code:	**VLPCC1002**	**Credit**	**3**
Contact Hours:	3 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Evaluation 40 Marks	End-sem. Examination 60 Marks	

Pre-requisites:

MOSFET, Digital Circuits, CMOS design

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-Sem. Evaluation	Internal	40
2.	End Semester Examination	External	60

Course Objectives	
1	To understand the basic concepts and models in SoC
2	To explore Micro-programmed Architectures and SoC modeling
3	To explore features of simulation and synthesis of RTL intent
4	To learn recent trends in SoC design

Course Outcomes: Students will be able to	
1002.1	Learn Design flow graphs and flow modeling
1002.2	Understand SoC modeling and interfacing
1002.3	Gain knowledge of SoC memory system design, embedded software and energy management techniques for SoC design, SoC prototyping, verification, testing and physical design.
1002.4	Design , implement and test SoC

Topics covered:

Module I: (10 hrs.)

Basic Concepts: The nature of hardware and software, data flow modelling and implementation, the need for concurrent models, analyzing synchronous data flow graphs, control flow modelling and the limitations of data flow models, software and hardware implementation of data flow, analysis of control flow and data flow, Finite State Machine with data-path, cycle based bit parallel hardware, hardware model, FSMD data-path, simulation and RTL synthesis, language mapping for FSMD.

Module II: (10 hrs.)

Micro-programmed Architectures : limitations of FSM , Micro-programmed : control, encoding, data-path, Micro-programmed machine implementation , handling Micro-program interrupt and pipelining, General purpose embedded cores , processors, The RISC pipeline, program organization, analyzing the quality of compiled code, System on Chip, concept, design principles , portable multimedia system, SOC modeling, hardware/software interfaces , synchronization schemes, memory mapped Interfaces, coprocessor interfaces, coprocessor control shell design, data and control design, Programmer's model.

Module III: Logic design (10 hrs.) RTL intent : Simulation race, simulation-synthesis mismatch, timing analysis, timing parameters for digital logic, factors affecting delay and slew, sequential arcs, clock domain crossing ,bus synchronization , preventing data loss through FIFO, Importance of low power, causes and factors affecting power, switching activity, simulation limitation, implication on synthesis and on backend.
Module IV: Advanced trends (10 hrs.) Research topics in SOC design: A SOC controller for digital still camera, multimedia IP development image and video CODECS, SoC memory system design, embedded software, and energy management techniques for SOC design, SOC prototyping, verification, testing and physical design.

Text Books:

1. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co-design", Springer Publications.
2. Sanjay Churiwala, SapanGarg , "Principles of VLSI RTL Design A Practical Guide", Springer Publications.

Reference Books:

1. Youn-Long Steve Lin, "Essential Issues in SOC Design, Designing Complex Systems-on- Chip", Springer Publications.
2. Wayne Wolf, "Modern VLSI Design Systems on Chip", Pearson Education.
3. Rajanish K. Kamat, Santhosh A. Shinde, Vinod G. Shelake, "Unleash the System On Chip using FPGAs and Handel C", Springer Publications.

M. Tech First Year Electronics and Telecommunications (2023 Course)
Testing and Verification of VLSI Circuits

Course Code:	**VLPCC1003**	**Credit**	**4**
Contact Hours:	4 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Evaluation 40 Marks	End-sem. Examination Activity based 60 Marks	

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-Sem. Evaluation	Internal	40
2.	End Semester Examination (Activity based)	External	60

Course Objectives

1	To introduce design process in VLSI
2	To understand the logical and Fault simulation models
3	To learn techniques for design of testability
4	To study hardware and software verification issues for testing

Course Outcomes: Students will be able to

1003.1	To accept challenges in VLSI Testing at different abstraction levels.
1003.2	Understand fault models for generation of test vectors.
1003.3	To enhance testability of a circuit.
1003.4	To identify characteristics of verification methods

Topics covered:

Module I: (10 hrs.)
Introduction to the concepts and techniques of VLSI (Very Large Scale Integration) design verification and testing,VLSI testing process and test equipment, test economics and product quality, fault modeling, testing and verification in VLSI design process.

Module II: (10 hrs.)
Test methods, logic and fault simulation, modeling circuits for simulation, algorithms for true-value simulation, algorithms for fault simulation, statistical methods for fault simulation, testability measures , combinational circuit test generation, sequential circuit test generation, memory test.

Module III: (10 hrs.)
Design for testability, Scan and Boundary scan architectures, Built-in Self-test (BIST) and current-based testing, analog test bus standard.

Module IV: (10 hrs.)
System test and core-based design, ATPG, Embedded core test fundamentals. Design verification techniques based on simulation, analytical and formal approaches. Functional verification. Timing verification. Formal verification. Basics of equivalence checking and model checking. Hardware emulation.

Text Books:

1. Bushnell M L, Agrawal V D, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers.
2. Abramovici M, Breuer M A and FriedmanA D, "Digital systems and Testable Design", JaicoPublications .

Reference Books:

1. Crouch A L, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall.
2. Kropf T, "Introduction to Formal Hardware Verification," Springer Publications.

M. Tech First Year Electronics and Telecommunications (2023 Course) ASIC Design			
Course Code:	**VLPCC1004**	**Credit**	**3**
Contact Hours:	3 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Evaluation 40 Marks	End-sem. Examination 60 Marks	

Pre-requisites: VLSI design, different software tools, basics of CMOS

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-Sem. Evaluation	Internal	40
2.	End Semester Examination	External	60

Course Objectives	
1	To gain knowledge of the process of designing application specific algorithm for ASIC
2	To synthesize designs in EDA tool environment
3	To learn design methodologies, simulation and verification
4	To learn issues in Mixed signal ASIC design

Course Outcomes: Students will be able to	
1004.1	To understand concepts and techniques of ASIC modeling and synthesis
1004.2	To perform static timing analysis, delay estimation and synchronization
1004.3	To learn ASIC Construction and testing techniques

Topics covered:

Module I: (10 hrs.)
ASIC Modeling and Synthesis :IC Design Technologies, Types of ASIC and Comparisons, ASIC Design Flow, Logic Synthesis, Simulation, EDA Tools, HDL Based logic Design and Test bench, library, logic level optimization.

Module II: (10 hrs.)
ASIC Physical Design :System Specifications, Architecture Design, Logic and Circuit Design, Physical Design, CAD Tools, System partitioning, Estimating ASIC Size, Power Dissipation, Partitioning Strategies, Floor planning, Placement, Routing, Design Reuse.

Module III: Logic design (10 hrs.)
ASIC Timing Analysis: Static timing analysis, Timing constraints, false path detection, Timing optimization, ASIC library design, Delay estimation, mixed mode design and simulation, SI issues.

Module IV: (10 hrs.)
ASIC Verification and Testing: Different Chip Test Methods, Fault Models, Scan Test, Partial Test, Digital scan standards, BIST architecture, Memory Testing, BILBO, Boundary Scan, Self Test, JTAG, ATPG. Mixed Signal ASIC Design: Mixed Signal ASIC Design, Practical aspects of mix analog digital design, Gate level mixed mode simulation. A brief introduction to signal integrity effects in ASIC design, Synthesis and Testing.

Text Books:

1. Smith Michael, "Application Specific Integrated Circuits" Pearson Education.
2. Soin R S, Maloberti F, Franca J, "Analogue-digital ASICs: circuit techniques, design tools and applications", IEE Publications.

Reference Books:

1. Singh Raminderpal, "Signal Integrity Effects in Custom IC and ASIC Designs", Wiley Publications.

M. Tech First Year Electronics and Telecommunications (2023 Course)
Mixed Signal IC Design (Elective II)

Course Code:	**VLPEC1006**	**Credit**	**3**
Contact Hours:	3 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Evaluation 40 Marks	End-sem. Examination 60 Marks	

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-Sem. Evaluation	Internal	40
2.	End Semester Examination	External	60

Course Objectives

1	To introduced Mixed Signal layout issues in circuit design
2	To explain the Architectures of ADC and DAC
3	To acquire knowledge on Modeling Data Convertors

Course Outcomes: Students will be able to

1006.1	Understand the mixed signal issues in circuit design
1006.2	Learn modeling different ADC and DAC
1006.3	Apply methods to improve SNR
1006.4	Explore the operation of delta-sigma/ sigma-delta converterand their issues

Topics covered:

Module I: (10 hrs.)
Analog versus discrete time signals, Converting analog signal to digital signal, Sample and hold characteristics, DAC specifications, ADC specifications, Mixed signal layout issues: floor planning, power supply and grounding issues, fully differential design/ matching, guard rings, shielding, interconnect considerations.

Module II: (10 hrs.)
DAC architectures: Resistor string, R-2R ladder networks, Current steering, Charge-scaling, Pipeline. ADC architectures: Flash, Pipeline, Dual slope, Successive approximation, Oversampling ADC.

Module III: (10 hrs.)
Data converter modeling: Sampling and aliasing: A modeling approach, Impulse sampling, AAF and RCF, Time domain description of reconstruction, The sample and hold, S/H spectral response, Circuit concerns for implementing S/H. Quantization noise, RMS quantization noise voltage, treating quantization noise as a random variable, calculating RMS quantization noise voltage from a spectrum.

Module IV: (10 hrs.)

Data converter SNR: Effective number of bits, Signal to noise plus distortion ratio, Spurious free dynamic range, dynamic range, SNR & SNDR, Clock jitter, Averaging to improve SNR, Spectral density view, Jitter and averaging, Relaxed requirements on AAF, Data converter linearity requirements, Adding noise dither to ADC input, Decimating filters for ADC. Decimating filters for ADCs, Interpolating filters for DACs. Noise-shaping data converters: First order noise shaping, Second order noise shaping, Noise shaping topologies: Higher-order modulators, Miltibit modulators, Cascaded modulators.

Text Books:

1. Baker R J, "CMOS: Mixed Signal Circuit Design", Second edition, Wiley IEEE Press Publications.
2. Baker R J, "CMOS: Circuit Design, Layout and Simulation", Second edition, Wiley IEEE Press Publications.
3. Allen, Phillip E., Holberg, Douglus R., "CMOS Analog Circuit Design", Oxford University Press Publications.

M. Tech First Year Electronics and Telecommunications (2023 Course)
High Speed IC (Elective II)

Course Code:	**VLPEC1006**	**Credit**	**3**
Contact Hours:	3 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Evaluation 40 Marks	End-sem. Examination 60 Marks	

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-Sem. Evaluation	Internal	40
2.	End Semester Examination	External	60

Course Objectives

1	To understand basic design aspects of high frequency circuits
2	To explain different characteristics of high speed logic families
3	To learn design issues of interconnects in High Speed Circuit Design

Course Outcomes: Students will be able to

1006.1	To acquire knowledge about High Speed VLSI Circuits Design.
1006.2	To identify the basic need of high speed digital logic families.
1006.3	To understand various types VLSI interconnections and to analyze various interconnection delay models.
1006.4	To acquire insights of nanotechnology circuits interconnections.

Topics covered:

Module I: (10 hrs.)
A brief history of high-frequency integrated circuits and its design, High-frequency circuits in wireless, fiber-opticand imaging systems.

Module II: (10 hrs.)
High-speed digital logic families, Design methodology for maximum data rate, Bi-CMOS MOS-HBT logic, Pseudo-CML logic, Other bipolar, MOS and Bi-CMOS CML, and ECL gates, CML/ECL gate layout techniques.

Module III: (10 hrs.)
Metal-Insulator-Semiconductor Microstrip Line Model of an Interconnection., Transmission Line Analysis of Single Level Interconnections, Transmission Line Analysis of Parallel Multilevel Interconnections, Very High Frequency Losses in a Microstrip Interconnection, Compact Expressions for Interconnection Delays, Interconnection Delays in Multilayer Integrated Circuits.

Module IV: (10 hrs.)

High Speed Circuit Design:High Speed Properties of logic gates-power, speed and packaging. Cross talk in solid ground and slotted ground planes, Near end and Far end cross talk. End terminators and cross talk in terminators, Vias and its characteristics. Stable voltage references, Connectors and cross talk due to connectors. Clock jitter and signal integrity mechanism for high speed link. Clock and power distribution related problems.

Text Books:

1. VoinigescuSorin, “High-Frequency Integrated Circuits”, Cambridge University Press.
2. Goel A K, “High-Speed VLSI Interconnections”, Second edition, Wiley-IEEE Press.
3. Nakhla M S, Zhang O J, “Modeling and Simulation of High Speed VLSI Interconnects”, Springer Publication.
4. Ludwig Reinhold, Bretchko Pavel, “RF Circuit Design Theory and Applications”, Pearson education.
5. Howard Johnson, Graham Martin, “High Speed digital Design-A Handbook of Black
6. Magic”, Pearson education.

M. Tech First Year Electronics and Telecommunications (2023 Course)
VLSI signal Processing (Elective II)

Course Code:	**VLPEC1006**	**Credit**	**3**
Contact Hours:	3 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	In-sem. Evaluation 40 Marks	End-sem. Examination 60 Marks	

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	In-Sem. Evaluation	Internal	40
2.	End Semester Examination	External	60

Course Objectives

1	To impart knowledge on the theoretical aspects of signal analysis and processing.
2	To explore DSP Processor architectures.
3	To understand DSP algorithms.
4	To elaborate real world DSP applications.

Course Outcomes: Students will be able to

1006.1	To design system with linear filters using DFT.
1006.2	To develop technical abilities of designing any applications with FIR and IIR filters
1006.3	To understand port algorithms on DSP Processor Platforms
1006.4	To design Adaptive filters Analyze filter structures

Topics covered:

Module I: (10 hrs.)
Signal Analysis and Processing: Discrete Fourier Transform, Fast Fourier Transform, Design of FIR Filters using windowing technique, Design of IIR Filters through Impulse invariance and bilinear transformation technique, Algorithms of Adaptive Filters, Design and Applications of Adaptive Filters.

Module II: (10 hrs.)
Introduction to Digital signal processing systems, MAC, Barrel shifter, ALU, Multipliers, Dividers, DSP processor architecture, Software developments, Selections of DSP processors, Hardware interfacing, DSP processor architectures: TMS 320C54XX, TMS 320C67XX, Blackfin processor: Architecture overview, memory management, I/O management, Real time implementation Considerations, Memory System and Data Transfer, Code Optimization.

Module III: (10 hrs.)
Representations of the DSP algorithms, Block diagrams, Signal flow graph, Data-flow graph, Dependence graph. Iteration bounds: Critical Path, Loop Bound, Algorithm to compute iteration bound, Longest Path Matrix (LPM).

Module IV: (10 hrs.)
Practical DSP Applications: Audio Coding and Audio Effects, Digital Image Processing, Two-Dimensional Filtering, Image Enhancement, DTMF generation and detection, FFT algorithms, Wavelet algorithms, Adaptive algorithms: system identification, inverse modeling, noise cancellation, prediction.

Text Books:

1. Woon-SengGan, Sen M. Kuo, "Embedded Signal Processing With the Micro Signal Architecture", Wiley-IEEE Press.
2. KuoSen M, Woon-SengGan," Digital Signal Processors: Architectures, Implementations and Applications", Prentice-Hall.
3. Proakis J G, Manolakis D G, "Digital Signal Processing ,Principles, Algorithms and Applications", Prentice-Hall.
4. Lawrence R. R, Bernard Gold, "Theory and Application of Digital signal Processing", Prentice-Hall.
5. ParhiKeshab , "VLSI Digital Signal Processing System", Wiley Publication

M. Tech First Year Electronics and Telecommunications (2023 Course) Lab Practice II			
Course Code:	**VLPCC1005**	**Credit**	**2**
Contact Hours:	4 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	TW 50 Marks	OR 50 Marks	

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	Term Work	Internal	50
2.	Oral	External	50

The laboratory work will be based on completion of minimum two assignments/experiments confined to the courses of 2nd semester of each subject. (**Laboratory Assignments/Experiments**)

Subject: ACD

1. To design cascode current mirror for output current of 100 µA. Prepare layout and simulate. Comment on output resistance.
2. To design, prepare layout and simulate CMOS differential amplifier for CMRR of 40 dB. Comment on ICMR.
3. To design, prepare layout and simulate multistage CMOS RF amplifier in 90 nm technology for voltage gain of 60 dB, bandwidth of 100 MHz, and source impedance of 50 Ω.
4. To design CMOS RF amplifier for voltage gain of 60 dB. Suggest and design suitable technique to enhance the bandwidth. Simulate each added technique step by step. Comment on the improvement resulted each time. Prepare layout of the final schematic and simulate.
5. List the sources of cross talk. Explore in detail, the existence of cross talk in each case. Explain the mitigation techniques. Prepare case study for one of them. Verify the cross talk and its mitigation through simulation.

Subject: SOC

1. Design, simulate and implement FSM on PLD for detection of either of input sequence X = … 1001. .....or …1101… sequence and set output flags Y = "1" & Z="1" respectively. What is effect on area, speed, fan out and power by implementing this design using different state encoding styles?
2. Design and implement MOD4 counter on PLD and verify multi-clock operations by probing logic analyzer

Control bits	Count update after every sec.

00	0.25 sec
01	0.5 sec
10	1 sec
11	4 sec

Why gated clock is not preferred in digital design? Write Verilog code to implement CMOS layout which will generate glitch also design a RTL by Write VHDL will generate glitch and also measure it using electronic test equipment.

3. Implement temperature logging system as a co-design by Interfacing FPGA &μC 8051 as follows :

   i. LM 35 interfaced with ADC
   ii. ADC interfaced with FPGA
   iii. FPGA interfaced with μC 8051
   iv. μC 8051 is interfaced with LCD

4. To display real-time room temperature. If temperature is greater than 250 C Bi-colors LED should change its normal. Green color to RED color via opto-isolator by actuation of relay

Subject: TVVC

1. Write VHDL/Verilog code for MUX -D scan cell and Level Sensitive/edge triggered MUX – D scan cell.
2. Write a VHDL/Verilog code to realize functioning of clocked scan cell and LSSD scan cell design.
3. To develop an exhaustive test bench for lower level combinational designs:
   a. Adder and
   b. Multiplexer. To prepare a complete Test vector set for all possible stuck at faults parity checker where the data word is of 2-bit.

Subject: ASICD

1. Write HDL code to simulate, synthesis, and place & route memory on PLD. Check results and also write the test bench.
2. Write HDL code to simulate, synthesis, place & route FIFO on PLD. Check results and also write the test bench.
3. Draw CMOS layout & simulate shift register by applying DRC's of appropriate foundry using backend tool and check the output.
4. Draw CMOS layout & simulate 16:1 MUX by applying DRC's of appropriate foundry using backend tool and check the output.
5. Simulate Stuck at fault model of given function.

Subject: Mixed Signal IC Design (Elective 2)

1. Plot ideal transfer curves for 3 bit and 4 bit DAC, using VRef = 5V and 3V. Find the resolution for a DAC if the output voltage is desired to change in 1 mV increments.
2. For 3 bit ADC, VRef = 5V, Plot ideal transfer curve and quantization error.
3. Plot transfer curve and quantization error by shifting entire transfer curve of example 2, left by 1/2 LSB and calculate DNL.

4. Design and simulate anti-aliasing filter with two input sine waves having frequencies 4 MHz and 40 MHz.
5. Design and simulate sample and hold circuit, with 8 MHz sine wave sampled at 100 MHz.
6. Calculate SNR and plot ADC input and DAC output for cascaded 8 bit ADC and DAC operated on VDD=1.5 V, Vin = 24 mV (0.75VPP) and Sampling frequency = 100 MHz.

Subject: High Speed ICs (Elective 2)

1. Simulate RC circuit and comment on transient response.
2. Simulate startup model of RLC.
3. Simulate a transmission line to evaluate VSWR, reflection coefficient parameters considering different loading considerations using analog simulation tool.
4. Plot stability circle, for given values of S parameters

Subject: VLSI Signal Processing (Elective 2)

1. Design and simulate N point FFT by targeting DSP processor platform.
2. Design and simulate N tap FIR filter by targeting suitable DSP processor platform.
3. Design and simulate LMS adaptive filter.
4. Design a system for DTMF signal detection. Write a program to detect the DTMF signal using Goertzel algorithm
5. Performance comparison of different filter structure.
6. Record a speech file in your own voice with sampling frequency of 8000 Hz. Design a system to decompose a speech signal using Daubechies wavelet using wavelet packet decomposition. Write a program to implement the system and plot the speech signal passed via each wavelet filter

M. Tech First Year Electronics and Telecommunications (2023 Course) Human Values in ethics and Education			
Course Code:	**VLHSM1007**	**Credit**	**1**
Contact Hours:	1 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	TW 25		

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	Term Work	Internal	25

Course Objectives	
1	To acquaint students about self-development.
2	To inculcate personality and behavior development within them.

Course Outcomes: Students will be able to	
1007.1	To introduce the students about self-awareness and self-development.
1007.2	To acquaint the students with human rights.

Topics covered:

Module I: (8 hrs.)
Values and Self Development-Social values and individual attitudes, Work ethics, Indian vision of humanism, Moral and non-moral valuation, Standards and principles, Value judgments. Importance of cultivation of values, Sense of duty, Devotion, Self-reliance, Confidence, Concentration, Truthfulness, Cleanliness, Honesty, Humanity, Power of faith, National unity, Patriotism, Love for nature, Discipline.

Module II: (8 hrs.)
Personality and Behavior Development- Soul and scientific attitude, God and scientific attitude, Positive thinking, Integrity and discipline, Punctuality, Love and kindness, Avoiding fault finding, Free from anger, Dignity of labor, Universal brotherhood and religious tolerance, True friendship, Happiness vs. suffering love for truth, Aware of self-destructive habits, Association and cooperation, Doing best, Saving nature.

Module III: (8 hrs.)
Human Rights- Jurisprudence of human rights nature and definition, Universal protection of human rights, Regional protection of human rights, National level protection of human rights, Human rights and vulnerable groups. Legislative Procedures- Indian constitution, Philosophy, fundamental rights and duties, Legislature, Executive and Judiciary, Constitution and function of parliament, Composition of council of states and house of people, Speaker, Passing of bills, Vigilance, Lokpal and functionaries References

Text Books:

1. Chakraborty, S.K., Values and Ethics for Organizations Theory and Practice, Oxford University Press, New Delhi, 2001.
2. Kapoor, S.K., Human rights under International Law and Indian Law, Prentice Hall of India, New Delhi, 2002.

3. Basu, D.D., Indian Constitution, Oxford University Press, New Delhi, 2002.
4. Frankena, W.K., Ethics, Prentice Hall of India, New Delhi, 1990.
5. Meron Theodor, Human Rights and International Law Legal Policy Issues, Vol. 1 and 2,Ox ford University Press, New Delhi, 2000.

M. Tech First Year Electronics and Telecommunications (2023 Course) Disaster Management			
Course Code:	**VLHSM1007**	**Credit**	**1**
Contact Hours:	1 Hrs/week (L)	**Type of Course:**	Lecture
Examination Scheme	TW 25		

Course assessment methods/tools:

Sr. No.	Course assessment methods/tools	External/ Internal	Marks
1.	Term Work	Internal	25

Course Objectives	
1	To introduce to concepts of hazards.
2	To inculcate students to various disaster impact's.
Course Outcomes: Students will be able to	
1007.1	To classify different disasters methods.
1007.2	To aware disaster risks and role of government in it.

Topics covered:

Module I: (8 hrs.)
Introduction: Concepts and definitions: disaster, hazard, vulnerability, risk, capacity, impact, prevention, mitigation). Disasters classification; natural disasters (floods, draught, cyclones, volcanoes, earthquakes, tsunami, landslides, coastal erosion, soil erosion, forest fires etc.); manmade disasters (industrial pollution, artificial flooding in urban areas, nuclear radiation, chemical spills etc); hazard and vulnerability profile of India, mountain and coastal areas, ecological fragility

Module II: (8 hrs.)
Disaster Impacts :Disaster impacts (environmental, physical, social, ecological, economic, political, etc.); health, psycho-social issues; demographic aspects (gender, age, special needs); hazard locations; global and national disaster trends; climate-change and urban disasters.

Module III: (8 hrs.)
Disaster Risk Reduction (DRR) : Disaster management cycle – its phases; prevention, mitigation, preparedness, relief and recovery; structural and non-structural measures; risk analysis, vulnerability and capacity assessment; early warning systems, Post-disaster environmental response (water, sanitation, food safety, waste management, disease control); Roles and responsibilities of government, community, local institutions, NGOs and other stakeholders; Policies and legislation for disaster risk reduction, DRR programmes in India and the activities of National Disaster Management Authority

Text Books:

1. http://ndma.gov.in/ (Home page of National Disaster Management Authority).
2. http://www.ndmindia.nic.in/ (National Disaster management in India, Ministry of Home

Affairs).

3. PradeepSahni, 2004, Disaster Risk Reduction in South Asia, Prentice Hall.
4. Singh B.K., 2008, Handbook of Disaster Management: techniques & Guidelines, Rajat Publication.
5. Ghosh G.K., 2006, Disaster Management,APH Publishing CorporationKapoor, S.K., Human rights under International Law and Indian Law, Prentice Hall of India, New Delhi, 2002.