Guidelines on B. E. Project

By

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Prepared By: Ms. Shobha Nikam

Marks (Credits: 8/44)

Department	Phase-I Marks	Phase-II Marks	Total	% Marks
Electrical	50(OR)	50(TW) 100(OR)	200	13.33
E&TC	50(OR)	150(TW) 50(OR)	250	16.67
Electronics	50(OR)	150(TW) 50(OR)	250	16.67
Computer	50(OR)	100(TW) 50(OR)	200	13.33
Information Technology	50(OR)	50(TW) 100(OR)	200	13.33
Instrumentation	50(TW)	100(TW) 50(OR)	200	13.33

Objectives of the BE Project

- To develop student's knowledge for **solving technical problems.**
- To provide an opportunity to **learn about new ideas and concepts.**
- To **analyze, design and evaluate** Engineering System.
- To provide an opportunity to **work in team.**
- To develop the **leadership quality.**
- To improve **Written and Verbal Communication skills**.

Course Outcomes

After completion of this course students will be able to

1. Apply the knowledge of mathematics, science and engineering fundamentals to the solution of complex engineering problems.

2. Implement practically ideas/real time industrial problems/ current application of respective/ multidisciplinary engineering branches .

3. Apply project management skill to design system/product by taking into consideration different issues such as safety, ethics, social, health, legal, cultural and cost standards.

Course Outcomes

4. Use different modern tools and equipments like LabView, Xilinx, MATLAB, multisim, Keil, NS-II, spectrum Analyzer, Logic analyzer, MSO, Vector Network analyzer etc.

5. Participate in National/International paper presentation/publication/project competition activities.

6. Prepare project Report (proposals) and present their project work in English.

B.E. Projects-Work Program

Sr. No.	Schedule	Target Dates
1	Finalization of project and submission of synopsis.	19/08/2020
2	Final approval of project Title	24/08/2020
3	Finalization of block diagram and literature survey	05/09/2020
4	Presentation based on the idea of their project and study of at least three existing systems.	08/09/2020
5	Finalization of circuits/ system hardware/ software algorithm	26/09/2020
6	Component list (Budgeting of System)	03/10/2020
7	Presentation based on the work carried out (analysis and design)	08/10/2020
8	Submission of pre-report(Project part-I)	01/11/2020
9	Bread board testing and prototype work	15/11/2020
10	Circuit layout and PCB	15/12/2020
11	Hardware assembly	30/01/2021
12	Presentation based on the completion of design and implementation	08/02/2021
13	To send paper to only International Journal (UGC approved) and participation in project Competition.	01/03/2021
14	Presentation based on the complete project including results and analysis.	24/02/2021
15	Report Submission.	29/03/2021

Computer Department

Sr. No.	Schedule	Target Dates
1	Registration of Project Teams	20/08/2020
2	Submission of Project Proposal /Synopsis	27/08/2020
3	Finalization of projects & allotment of guide	4/09/2020
4	Project presentation-I	11/09/2020
5	Submission of final Proposal	21/09/2020
6	Design Diagrams (UML)	07/10/2020
7	Submission and Internal Evaluation of project report (Sem-I)	30/10/2020
8	Coding and Implementation	27/02/2021
9	Validation and Testing	15/03/2021
10	Report Submission.	15/04/2021

Format of Synopsis

- Cover page as per the format of first page of report.
- Introduction
- Brief Literature Survey
- Problem Statement
- Objectives
- Methodology
- Block Diagram
- Expected Results
- Time schedule for completion of project.
- References (at least 5-6 references)
- Signature of Student and Guide
- Maximum Number of pages for synopsis = 2 to 3

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Department Of Electronics and Telecommunication Engineering

SYNOPSIS

TITLE:

GROUP NO.:

GUIDE:

ACADEMIC YEAR:

GROUP MEMBERS:

Roll No	Name	Email ID	Mobile	Signature

1. INTRODUCTION:

The aim of the project is to

. In our project, we are basically concentrating on following applications such as:

- To.
- To.
-

Security System:

2. LITRATURESURVEY:

[1]

[2]

[3]

SUMMARY OF LITERATURE SURVEY:

From the above literature survey it can be summarized that it is possible for

The plan is to. There are various drawbacks

[1]

[2]

3. PROBLEM STATEMENT:

4. OBJECTIVES:

1.
2.
3. .

5. METHODOLOGY

6. BLOCK DIAGRAM:

7. EXPECTED RESULTS:

8. TIME SCHEDULE FOR COMPLETION OF PROJECT (TABULAR FORM):

9. REFERENCES:

1.
2.
3.
4. .

Student Sign

1.
2.
3.

Guide Sign

Project Phase-I Exam

- Examination : November / December
- Report format same as phase-II is to be followed.
- 50% work completion is expected.

Format of the Project Report (Phase-II)

Page number	Preface
--	Vision, Mission, CO and PO.
--	Title Page
i	Certificate Page
ii	Certificate from Company (Sponsored)
iii	Abstract
iv	Index Page
v	Acknowledgements
vi	List of Tables
vii	List of Figures
viii	List of Abbreviations
	Note: For these pages the page numbers should be in small roman numbering form.

Main Body of project report

CHAPTER NO.	CONTENTS
1	Introduction (2-4 pages)
2	Literature Survey
3	Aim & Objectives
	3.1 Aim
	3.2 Objectives
	3.3 Methodology
	3.4 Specifications of the System
4	Block diagram of the System and its explanation./ Architecture (Comp/IT)
5	Hardware Design (if any)
6	Software Design (if any)
7	Tests and Results.
8	Conclusion
	References

Main Body (COMP/IT)

Chapter. No.	Title of Chapter
1	Introduction
2	Literature Survey
3	Software Requirements Specification
4	System Design
5	Project Plan
6	Project Implementation
7	Software Testing
8	Results
9	Conclusions
10	References

Appendix

Sr. No.	Contents
A1	Bill of material.
A2	Important Datasheets.
A3	Project participation certificates.
A4	Hard copy of published paper at UGC approved International Journal with DOI number and Certificates. (To publish paper in scopus indexed journal reward of Rs. 4000/- will be given)
A5	Plagiarism report of project.
A6	Project monitoring sheet/ Log Book
A7	Self evaluation sheet
A8	CD must be attached at the end of the report. CD must contain final report, plagiarism report, project exhibition participation certificates, published paper, software codes, video of working of project.

Format of Title Page

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A
PROJECT REPORT ON

LOW COST 4-CHANNEL LOGIC ANALYZER

SUBMITTED TO THE SAVITRIBAI PHULE PUNE UNIVERSITY, PUNE IN THE PARTIAL FULFILLMENT FOR THE AWARD OF THE DEGREE

OF

BACHELOR OF ENGINEERING IN

Electronics and Telecommunication

BY

AJINKYA PASALKAR (B150253102)
ASHISH KUMAR MANDA (B150253010)
ASHUTOSH WAIKUL(B150253011)

UNDER THE GUIDANCE OF

D.r.P.B.MANE

Department of Electronics and Telecommunuication

AISSMS Institute of Information Technology, Pune.

2018 - 2019

Format of Certificate

CERTIFICATE

This is to certify that the Project Entitled

LOW COST 4-CHANNEL LOGIC ANALYZER

Submitted by

AJINKYA PASALKAR (B150253102)
ASHISH KUMAR MANDA (B150253010)
ASHUTOSH WAIKUL(B150253011)

Is a bonafide work carried out by them under the supervision of D.r.P. B.MANE and it is approved for the partial fulfilment of the requirement of Savitribai Phule Pune University for the award of the Degree of Bachelor of Engineering (Electronics and Telecommunication)

This project report has not been earlier submitted to any other or university for the award of any degree or diploma.

D.r.P.B.Mane
Principal and Internal guide
AISSMS Institute of Information Technology, Pune

Dr. M. P. Sardey
H.O.D
Department of E and TC

External Examiner

Date: 8/6/2019
Place: AISSMS IOIT, Pune.

Abstract Contents

- Introduction.
- Review of existing work with Limitations.
- Work carried out .
- Comment on Result.

Example: Abstract

Importance/ Need	Advancement in satellite communication applications has increased demand of miniaturization in broadcasting and telecommunication networks. Transceivers are widely used to accomplish broadband requirements of satellites. Phase locked loops(PLL) are used in transceivers for carrier generation. Generation of clean signal is a primary goal of any synthesizer. In PLL Voltage Controlled Oscillator(VCO) is a crucial element because it contributes more phase noise compared with other PLL blocks.
Existing Work	Various PLL ICs are available but in wide band PLL ICs all components are not implemented on same chip because of parasitic effect.
Methodology	This paper presents parasitic aware methodology for circuit design using 90nm CMOS process. Centre frequency, output amplitude, tuning range, gain and tuning linearity are considered as important parameters in VCO design.
Work Done	Design and implementation of LC-tank VCO using only NMOS topology is presented.
Quantitative Results	The implemented VCO generates 15GHz carrier frequency. Noise performance of Voltage Controlled Oscillator (VCO) is evaluated using Process Voltage Temperature (PVT) variation analysis and corner analysis and results are compared with existing work. Implemented VCO gives phase noise of -114.4dBc/Hz @1MHz offset, PSS of 9.95dBm with 2V swing.

How to Write Introduction

- Information about the latest trends/ achievements of the technology in which you have done your project.
- Information about the work carried out.
- A brief overview of the rest of the chapters.

Continued

5. A brief overview of the rest of the chapters must be included at the last paragraph of introduction as follows:

Chapter 2 presents Auditory features based on Gamma-tone filter-bank. Mel-scale and Bark-scale based Gamma-tone features are brieflydiscussed in this Chapter. Also experimentation has been carried out to evaluate the performance.

Chapter-3 reviews 1-D two channel FBs and addresses the problems with recently designed two-channel FBs. The two-channel FB problem formulates using three step ladder structure (THFB). The properties of this proposed THFB have been discussed.

In Chapter-4, the proposed class of THFB has been used in iris recognition system by investigating its properties to extract the discriminating iris features.

The construction of DWFB and RDWFB has been described in Chapter-5. This chapter also discussed the iris feature extraction algorithm based on a combined DWFB and RDWFB.

The report is concluded in Chapter-6.

Literature Survey

Find the latest material relevant to the project topic which is being explored.

1. Identify the "big names or researchers" and best publications in your working area.

   (papers or thesis will be most helpful for developing the project.)

1. Collect the most recent books, most popular publications from IEEE Transactions, Elsevier, Springer.

3. The minimum number of the papers to be collected is between Ten (10) to Twenty (20).

Literature Survey

- Explain each paper in one paragraph that should include following points:

1. Summarize all major points of your selected paper i.e. new work, results, its conclusion (Findings and conclusion)

2. Write the strengths and limitations of your selected paper.

3. Cite this paper by numbering inside the square bracket [].

4. Make comparisons of the selected papers and give technical comments.

5. Summary of comparison is to be given in a tabulated form in the last page.

Example to cite and review the paper if contains two authors

Pawar and Mane [2] highlighted importance of design of indigenous single chip, wide band, high frequency PLL IC for satellite communication applications. The output characteristics of PLL based frequency synthesizer are discussed which includes Tuning Range of frequency, Phase Noise and Frequency Resolution. The paper compares different topologies for low phase noise Integer-N phase locked loop in Ku band (12GHz-18GHz). The best topology suitable for wide band PLL is suggested considering phase noise as primary element and area and power consumption as secondary because the uncertainty of a synthesizer's output can be measured by its phase noise or spur level at a certain frequency offset from the desired carrier frequency.

[2]Shobha N. Pawar and Dr. Pradeep B. Mane, "Wide band PLL frequency synthesizer: A survey", IEEE, 2017 International Conference on Advances in Computing, Communication and Control (ICAC3), Dec-2017, DOI: 10.1109/ICAC3.2017.8318773

Example to cite and review the paper if contains more than two authors

Pawar *et al.* [2] highlighted importance of design of indigenous single chip, wide band, high frequency PLL IC for satellite communication applications. The output characteristics of PLL based frequency synthesizer are discussed which includes Tuning Range of frequency, Phase Noise and Frequency Resolution. The paper compares different topologies for low phase noise Integer-N phase locked loop in Ku band (12GHz-18GHz). The best topology suitable for wide band PLL is suggested considering phase noise as primary element and area and power consumption as secondary because the uncertainty of a synthesizer's output can be measured by its phase noise or spur level at a certain frequency offset from the desired carrier frequency.

Chapter 3
LITERATURE SURVEY

[1] Roland Szabó and Aurel Gontean presented a new approach for programming acquisition cards. The acquisition card is can be used to generate the signal generation and signal acquisition. The PC has many acquisition cards that are already built in. One acquisition card which can be programmed is the LPT or the parallel printer port. With this port, generation and acquisition of digital signals can be made possible and with help of Lab Windows. This system requires only male connector with wires as a hardware to connect input signal to PC and a correct computer program. However, this approach totally depends upon the computer acquisition card, which can't be available every time.

[2] Jia Luo, proposed an idea which focuses on the design of the hardware circuit and the firmware for the USB interface chip, and the realization of the computer applications based on the USB interface. An information monitoring device between the On-board Unit and the Rode Side Unit used in the Dedicated Short Range Communication in the Electronic Toll Collection has been realized in this design. This system is divided into three main parts .The signal receiver module mainly realized the receiving and demodulation of the microwave signal. The digital processing module will filter and amplify the baseband signal in order to meet the demands of the analog-digital converter. The date transmission module mainly works on transferring the sampling data from the ADC to the USB able at a high speed via a complex programmable logic device. However, this approach may increase the speed of the execution, but this kind of approach is too costly.

[3] Ishtiak Ahmed Karim, this paper describes the design and development of a low-cost portable oscilloscope based on Arduino and Graphical Liquid Crystal Display (GLCD). This project is designed and developed to achieve the same functionality that traditional oscilloscopes have. An Atmel microcontroller is used for data acquisition which will then be displayed as a waveform on a GLCD screen as it would have appeared on a traditional CRT oscilloscope. The oscilloscope displays waveforms in real-time by reading a finite number of samples and storing them into its internal RAM. Once the memory is full the Microcontroller will stop sampling and transfer the data to the GLCD display. This handheld oscilloscope is very cheap, uses low power, generates low internal noise, uses very few components and easy to operate.

[4] Sujur Alagar and Ramalingam This paper presents the design and implementation of a Handheld Logic Analyzer. It is based on the FPGA to capture 9 channel digital data and the ARM7 processor as a master controller, which reads these 9-channel data from the FPGA and

Tabular Format

Table1. Review of papers

Sr. No.	Paper	Methodology	Remark
1.	Aniruddha C. Kailuke et al., "Design of Phase Frequency Detector and Charge Pump for Low Voltage High Frequency PLL", 2014 International Conference on Electronic Systems, Signal Processing and Computing Technologies, IEEE.	Tool: Tanner 13 Process: 0.18-µm CMOS.	Analyzes the blind zone in latch-based PFDs and proposes a technique that removes the blind zone caused by the pre charge time of the internal nodes.
2.	Te-wen liao et. Al. "Spur-reduction frequency synthesizer Exploiting randomly selected PFD", IEEE Transactions On VLSI Systems, Vol. 21, No. 3, March 2013	Process: TSMC 0.18-µm CMOS phase noise: −93 dBc/Hz @600-kHz Reference spurs: below −72 dBc.	The low-spur frequency synthesizer randomizes the periodic ripples on the control voltage of the voltage controlled oscillator to reduce the reference spur at the output of the PLL.
3.	Chun-wei Hsu et al., "A 2.2GHz PLL using a Phase-Frequency Detector with an Auxiliary Sub-Sampling Phase Detector for In-Band Noise suppression" , 978-1-4577-0223-5/11/$26.00 ©2011 IEEE	Process: 65-nm CMOS Noise improvement: -110dBc/Hz to -122 dBc/Hz.	PFD and a sub-sampling phase detector are combined to maintain the phase-frequency detection capabilities while simultaneously obtaining in-band noise suppression.
4.	Jerry Yau, "A High-Speed Frequency Acquisition PLL Using Phase Frequency Detector with Variable Gain.", 978-1-4244-7773-9/10/$26.00 ©2010 IEEE	Locking time improvement : 49% .	Multi-state phase frequency detector with variable gain is presented which can efficiently reduce the locking time.

Summary of Literature Survey

Summary of Literature Survey:

From the literature reviewed it is observed that the researchers have focused on phase noise, power optimization and parasitic free design of

PLL. Most of the work is about power optimization and very few researchers have focused on phase noise. In available ICs phase noise is as low as -134.5 dBc/Hz @1 MHz offset but all components are not integrated on same chip (VCO or loop filter are externally connected). Proposed work aims to design fully integrated indigenous PLL frequency synthesizer for entire ku band (12 GHz- 18 GHz) satellite communication for low phase noise, it also aims to mitigate severe tradeoff between the channel frequency spacing and frequency switching time. Topologies for various blocks have been finalized from the above literature.

Problem Statement/ Aim

Example1: (E&TC Dept)

- Design and develop a low cost 4- channel logic analyzer to sample at 1MHz.

Example2:(Computer Dept)

- Develop a system which helps to classify the gender using biometric thumb impression.

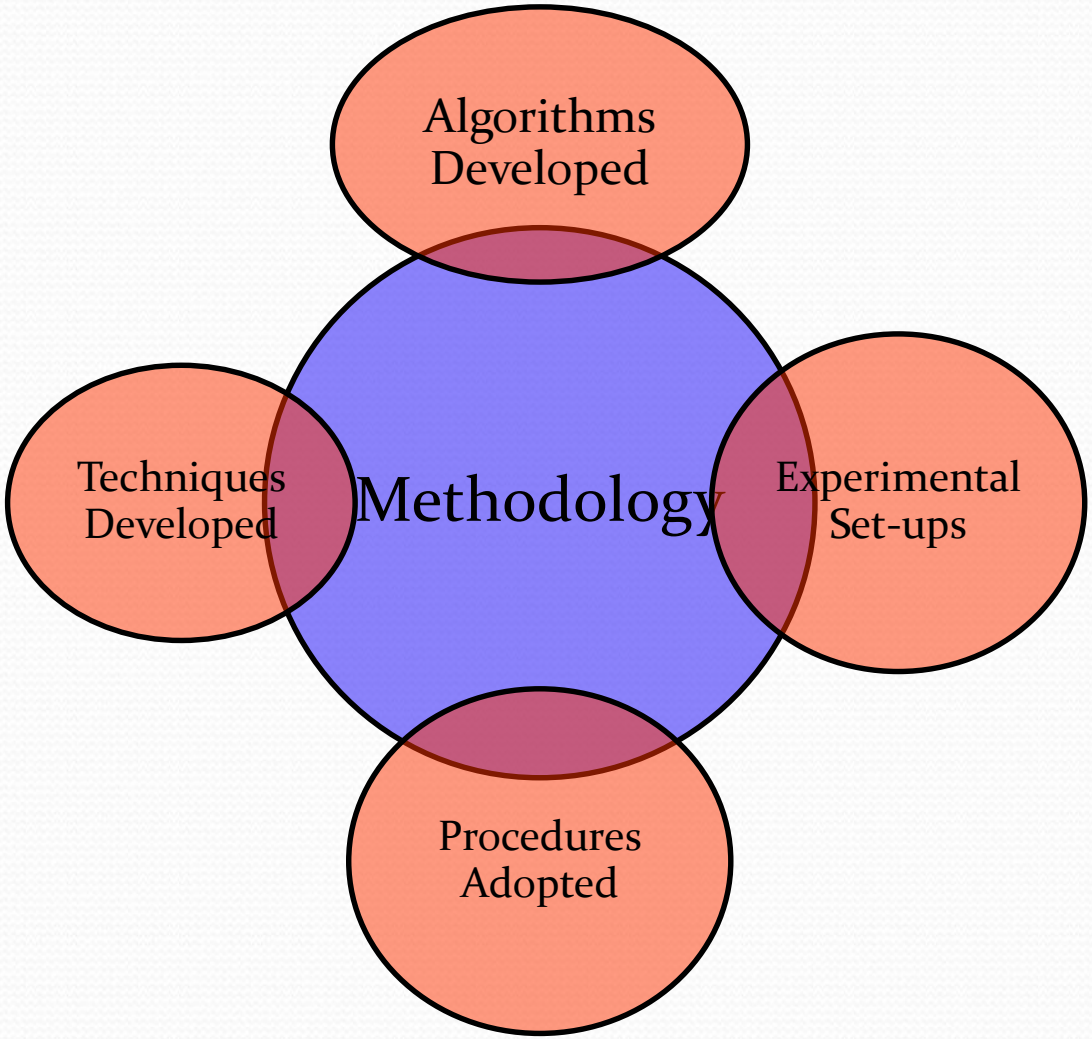
OBJECTIVES

- To study existing logic analyzers.
- To design and build logic analyzer.
- To develop algorithm for sampling and user interfacing.
- To test and validate the developed logic analyzer.

METHODOLOGY

- Method adopted to solve the problem.
- Give an overview of how can you carry out the project.
- Step-wise approach to the solution.

METHODOLOGY



Hardware/Software Design

- Describe the design of what you have created.
- Start with application block diagram and the components that make the block diagram.
- Give a description of the design of the component that make up the block diagram.
- Provide the implementation detail as necessary.
- Necessary to write the Algorithm of the Project.

Experimental Result and Analysis

- Include the Experimental Setup used for testing the system.
- Include the tables and graphs that shows your quantitative results.
- Write in sentences the thorough evaluation of the result being presented.
- Next, write the analysis on your obtained results.

How to Write Conclusion

- Summary of what the project has been achieved.
- Must include your quantitative results and logical analysis of the result presented in the project report.

How to Write References

- Number all the references.
- References has to be written in IEEE Transactions format.
- Use a chronological bibliography.
- Each listed reference in the bibliography must be cited in the text of the report.
- For a book, give the name(s) of author(s), title of the book, edition, chapter number, page number, publisher, location and year of publication.

How to Write References

- For a journal/conference paper, give the name(s) of authors, "title of paper", *name of journal/conference*, volume and issue number (for journal), page numbers, month and year of publication.

Example:

[1]K.D.shinde and Dr.P.B.Mane, "Augmenting rooftop solar energy penetration ratio with secondary distribution network using smart inverter for maximum power transfer capacity for subordinate grid- A review", Taylor & Francis, vol-41, issue-6, 2019, DOI:https://doi.org/10.1080/15567036.2018.1520353

[2]Shobha N. Pawar and Dr. Pradeep B. Mane, "Wide band PLL frequency synthesizer: A survey" , *IEEE 2017 International Conference on Advances in Computing, Communication and Control (ICAC3), Dec-2017, DOI: 10.1109/ICAC3.2017.8318773*

- For World Wide Web page, write the **URL**.

How to Write References

- For a book, give the name(s) of author(s), title of the book, edition, chapter number, page number, publisher, location and year of publication.

  e.g. Mane P.B. ,Bormane D.S. and Itkarkar R.R. "Television Engineering Audio and Video systems" 1st edition, cp.1-4, 2016, Wiley Publication.

- For World Wide Web page, write the **URL**.

Appendix

- Important Data sheet
- Lengthy Derivations
- Raw Experimental Observations

Should be presented in separate appendices which shall be numbered in Roman capitals (e.g. Appendix I, II, IV etc.)

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INSTITUTE OF INFORMATION TECHNOLOGY,PUNE

Department of Instrumentation and Control

B.E. Project Monitoring Sheet (SEM-I/II)

Name of Project:_____ Sponsored Company:_____

Name of Students: 1)_____ 2)_____3)_____

Internal Guide:_____ External Guide:_____

Sr. No.	Date	Work Done	Work to be Done	External Guide	Internal Guide

Self Evaluation sheet

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Department of Instrumentation and Control Engg.

Self Evaluation Sheet

Name of the Project	
Name of the Student	
Name of the Student	
Name of the Student	

File of Literature survey	Design	Implementation	Test & Results	Attendance on the Project Day	Work according to plan activity	Maintaining Log book	Paper presentation or participation	Project Exhibition Participation	Award , prize if any
(5)	(20)	(20)	(20)	(5)	(10)	(5)	(5)	(5)	(5)

Observation and Comments of Guide

Name of the student Sign of the Student Sign of Guide

1.

2.

3.

Note: The Evaluation will be verified by Project Evaluation Committee.

Instructions to Students for Preparing Project Report

- Project Presentation and Project-reports have to be **prepared in LaTeX Only. (Workshop will be conducted)**

- All the Figures of their Projects have to be prepared using **CorelDraw or AutoCad or Catia Softwares or Flash or RF Flow or google sketch.**

- All the **PCBs** or Analog/Digital Electronic circuits have to be simulated using **OrCad's schematic, Pspice or Multisim or Proetus.**

- **Plagiarism of report should be checked from library(Record will be maintained by library).**

Instructions to the Students

- Synopsis has to be submitted in the prescribed format.
- Students must maintain the **weekly progress notebook** (Log-book) in the specified format: [date of meeting, work assigned and carried out, future planning, decision taken, Sign of guide & students].
- Student can go to the company for the project work on the day(s) other than those mentioned in the time table only after taking the permission from guide and GFM.
- The attendance will be considered after submitting the attendance certificate from the respective company.

Instructions to the Students

- It is mandatory **to test and assemble the circuit in the college lab**
  before finalizing the artwork and layout of the PCB.

- Fabricated hardware should be enclosed in a **proper enclosure** designed by the students.

- Plagiarism is a very serious offence and, where proven against a student, may result in disqualification from the examination of the project.

- The final project reports are to be uploaded to AICTE portal.

Instructions to the Students

- The project report must be checked by their respective guide before **printing the final copy**.
- Each project group has to publish at least one paper at **International Journal till 27th February**. It is important to note that guide must approve the paper draft before student communicating their paper to the Journals.
- All the project groups have to participate at least in one **project competitions before 20th March.**
-

Instructions to the Students

- The system should be 100 % working as per their specification and objectives.
- Sponsorship letter of company is compulsory and is to be **submitted to project coordinator and project-guide.**
- Change of project /any modification in the aim/objective can be done only with the permission of the respective guide, project co-ordinator and HOD.
- University project examination may be conducted on any day including Saturday, Sunday and any other holiday. In this context, the project group has to submit the letter (NOC) to the Department regarding the conduction of examination on above days at their place.
- The company guide should be present at the time of examination.

Instructions to Guide and Project coordinators

- Based on students' presentations, the **record of mark-sheet** should be maintain by **project co-ordinator and project guide.**
- Every project guide will monitor the participation of their students in various project competitions.
- Collect all the certificates of students' participation in various project competitions.
- The format of **project report** will be displayed by **project co-ordinator**. Students must have to prepare their **project report** according to the displayed format.
- Mandatory for project guides to visit the company which has sponsored them the project group.
- The travel arrangement to the company should be made by the respective project group.

Mark sheet for evaluation

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Department of Instrumentation and Control Engineering.

Mark sheet for B. E. Project Presentation

Year 2009-10 (Semester II)

Sr. No.	Project Group	Project Topic Date of Presentation	Total Marks (50) Work Done(20), regular meet with Guide(05), Knowledge(15), Stage wise Implementation (10)	Guide Name & Sign
1 2	Darbha Srilakshmi S Jagtap Neha S Menon Malavika R Gunale Pravina A Pawar Pooja Ramesh	Development of intelligent langumuir through for nanoscience research Universal Environmental Meter		Mr. H. P. Chaudhari
3	Gokhale Madura B Kulkarni Ketki C	Visitor management system.		
4	Bhavsar Gauri P Anupama Kumari	Digital steganography for secret information retrieval		Mr. B.M.Kardile
5	Jadhav Neha M Kulkarni Bhavana A	Intelligent system for monitoring battery-bank health		
6	Doshi Snehal Mohan Thakur Prajakta P	Centralized monitoring of infusion pump.		
7	Akriti Priyadarshini Bopardikar Snehal A	Face recognition		Mr. N.S.Pathak
8	Kamat Deepti Rajiv Kulkarni Sayali P	DLC based controlled cabinet cooling with Vortex tube		

Format for Log-Book Assessment

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ASSESSMENT OF LOG-BOOK

Marks	Description
5 (Very Good)	• Have very frequent meetings with the guide. • Shows a genuine interest in the project and is exceptionally hard working and independent. • Project plan is exceptionally well prepared, systematic and appropriate. Conducts work according to plan and adapts well to changes.
4 (Good)	• Meets with the guide regularly. • Shows an interest in the project and is hardworking, and independent. • Project plan is well prepared, systematic and appropriate. • Mostly work is conducted according to plan and can adapt to changes.
3 (Fair)	• Meets with the guide once in a while, but not frequent enough. • Shows some interest in the project but in not fully committed. • Moderately hardworking, lacks inquisitiveness and is dependent on the guide half of the time. • Project plan needs improvement and should be more systematic and appropriate. • Work is not completely conducted according to plan and has some difficulty adapting to changes.
1 (Poor)	• Very seldom meets with the guide. • Shows little interest in the project and lacks commitment. Has issues with completing tasks, lacks and is dependent on the guide most of the time. • Project plan is flawed and needs to be more systematic and appropriate. • Work is not conducted according to plan and has major difficulty adapting to changes.
0 (Very Poor)	• Hardly ever meets with the guide. • Shows no interest in the project has major issues with completing tasks, shows no signs of inquisitiveness and is highly dependent on the guide. • Project plan is seriously flawed. • Seldom does work and cannot adapt to changes.

Format for Presentation Assessment

ALL INDIA SHRI SHIVAJI MEMORIAL SOCIETY'S
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ASSESSMENT OF PRESENTATION S BY GUIDES AND EXAMINERS

Marks	Description
5 (Very Good)	• Flawless presentation, exhibiting highly commendable skills. • Exceptionally well-prepared and attractive slides/poster that clearly covers the main aspects of the project. • Questions answered exceptionally well and with ease.
4 (Good)	• Impressive presentation, exhibiting commendable skills. • Well-prepared and attractive slides/poster that covers the main aspects of the project. • Questions answered well and rather convincingly.
3 (Fair)	• Average presentation. Skills require improvement. • Adequately prepared slides/preparation of slides/poster with important aspects of the project being left out. • Some questions could not be answered convincingly.
2 (Poor)	• Unimpressive presentation due to lack of skills. • Very little thought given to the preparation of slides/poster with important aspects of the project being left out. • Failed to answer most of the questions convincingly
1 (Very Poor)	• Seriously flawed presentation due to little or no skills. • No thought given to the preparation of slides /poster with most aspects of the project being left out. • Unable to answer the questions convincingly.

THANK YOU